Unit 11

Flip-Flops

Outline

- Introduction
- Set-Reset latch
- Gated D latch
- Edge-triggered D Flip-Flop
- Set-Reset Flip-Flop
- J-K Flip-Flop
- T Flip-Flop
- Flip-Flop with additional inputs
- Summary

Introduction (1/3)

Combinational: Output is a function of present inputs only

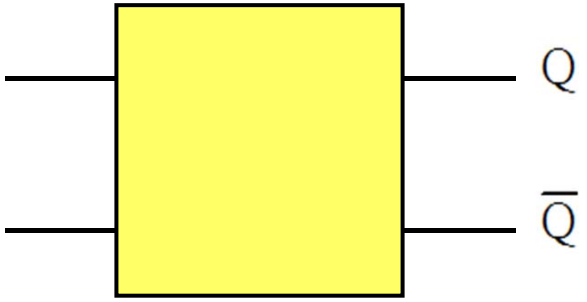
Sequential : Output is a function of both present and previous inputs

Circuit "remembers" previous history using

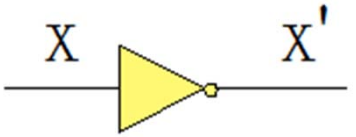
→ Flip-Flop (F/F): with clock input (on clock edge)

→ Latch : with no clock input (or on clock level)

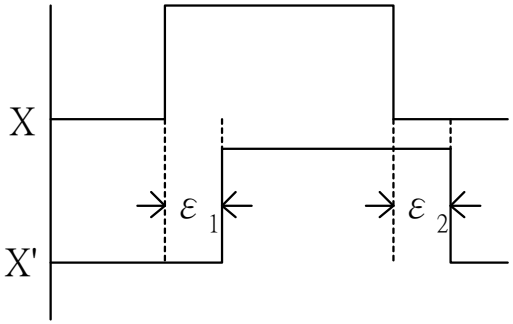
F/F: a memory device with 1 output, or 2 complementary outputs



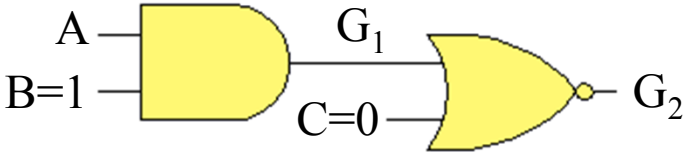
Introduction (2/3)

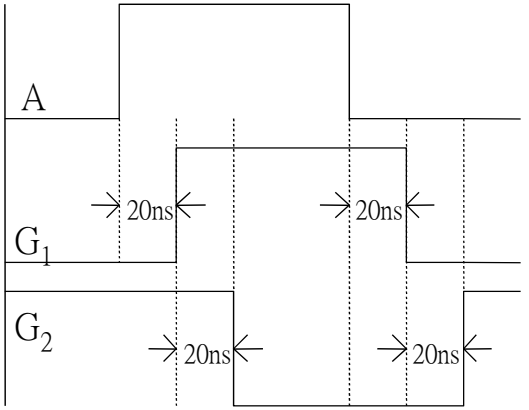


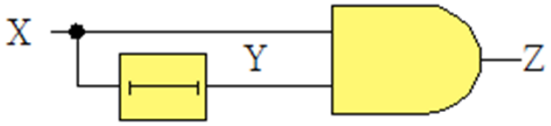
ε_1, ε_2 may be very small but still exist.



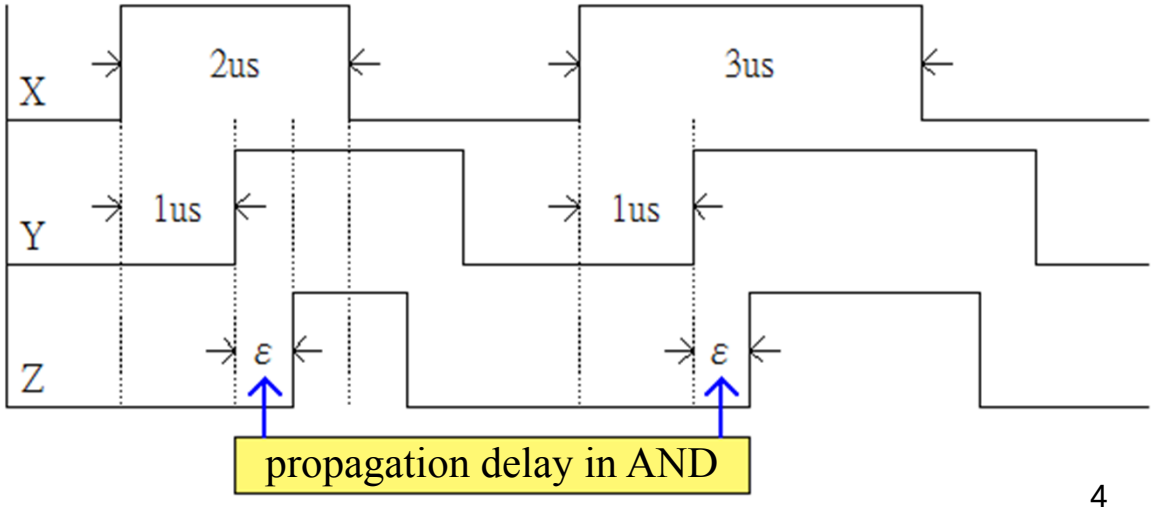
Timing







1us delay
due to wire length



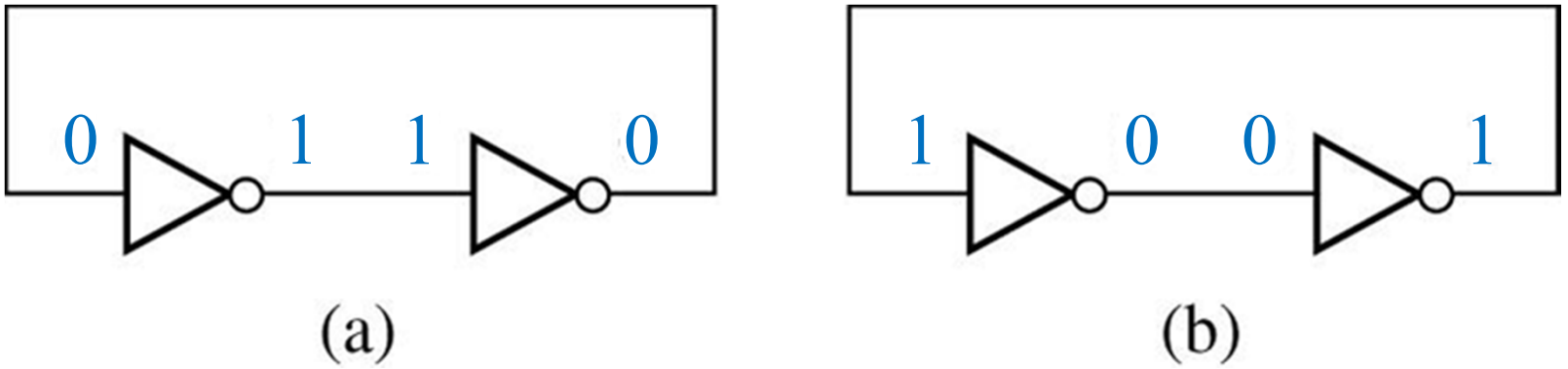
Introduction (3/3)

Timing in feedback network

One inversion (oscillatory)

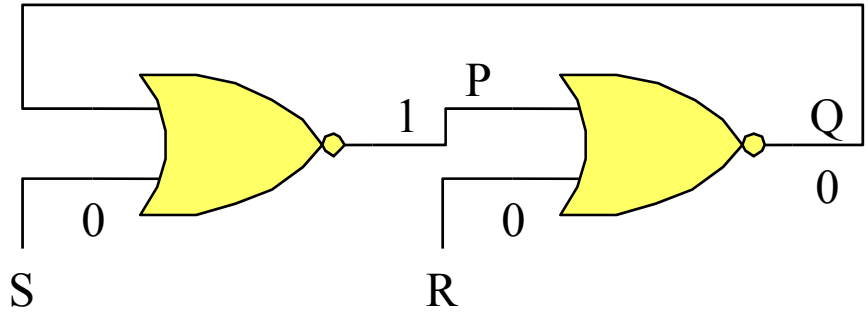
(a) Inverter with feedback (b) Oscillation at inverter output

Two inversions (stable)

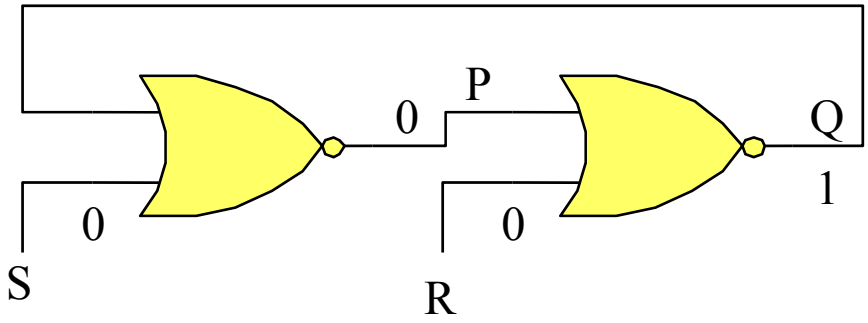


(a) (b)

Set-Reset Latch (SR Latch) (1/9)

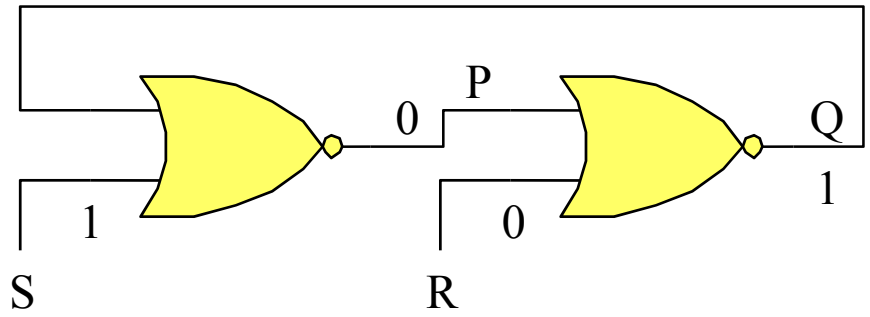


$S=R=0,\ Q^{+}=Q$



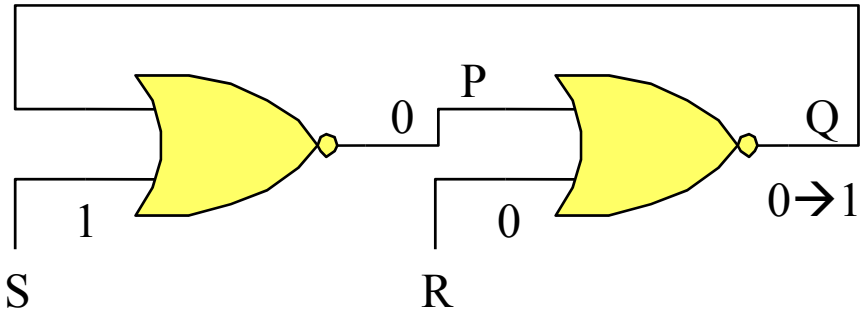
$P=Q'$

Set-Reset Latch (SR Latch) (2/9)



$S=1, R=0, Q=1, Q^{+}=1$

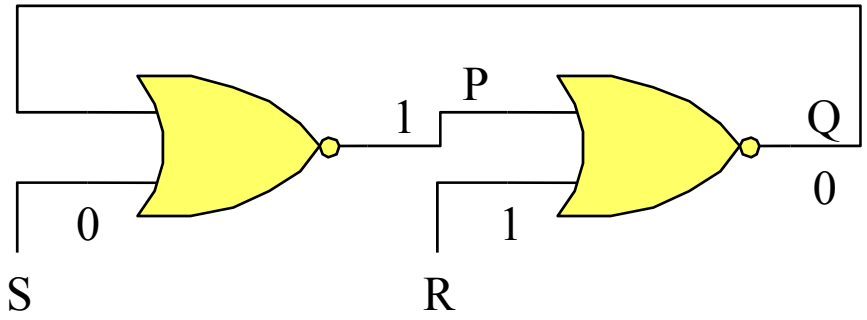
$P=Q'$



$S=1, R=0, Q=0, Q^{+}=1$

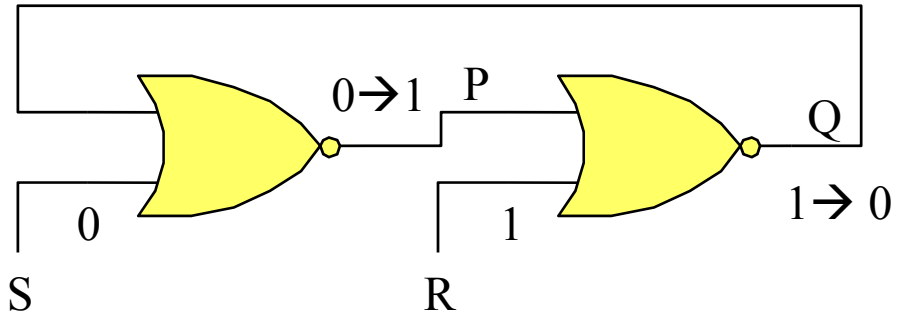
Set: $S=1, R=0, \rightarrow Q^{+}=1$

Set-Reset Latch (SR Latch) (3/9)



S=0, R=1, Q=0, Q^+=0

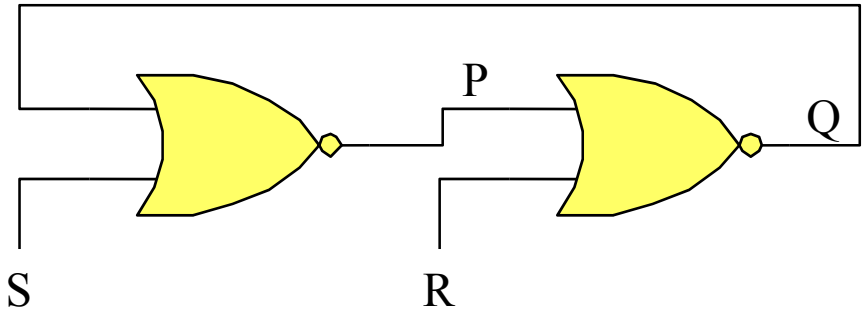
P=Q′



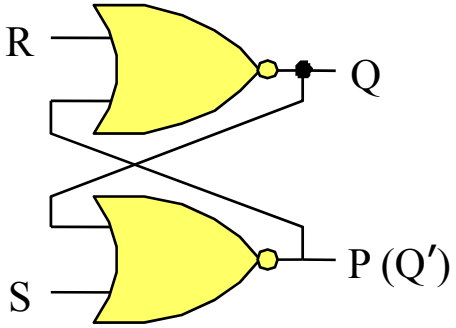
S=0, R=1, Q=1, Q^+=0

Reset: S=0, R=1, → Q^+=0

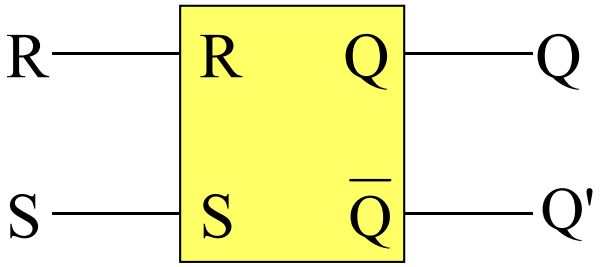
Set-Reset Latch (SR Latch) (4/9)



Original circuit

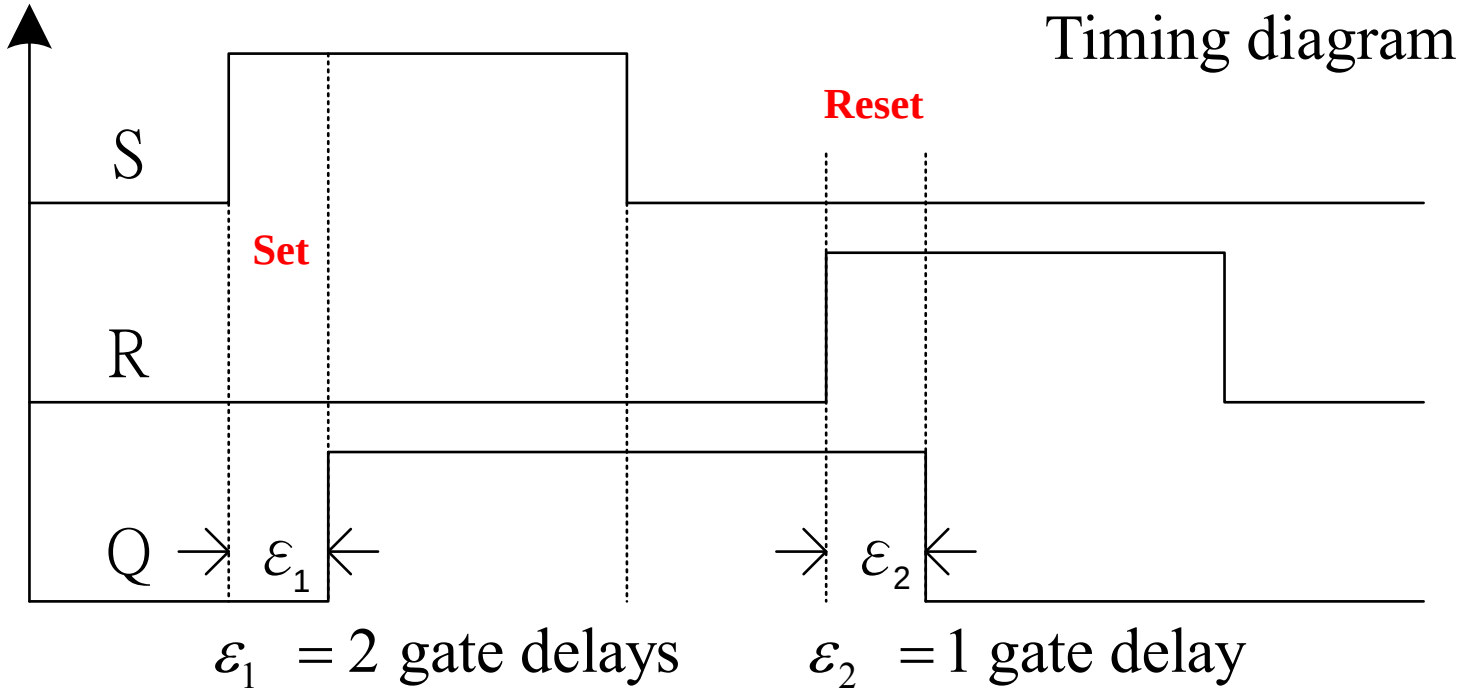


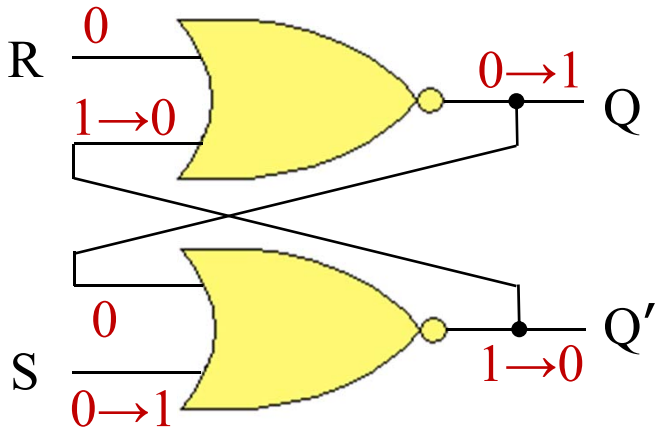
Restructured circuit



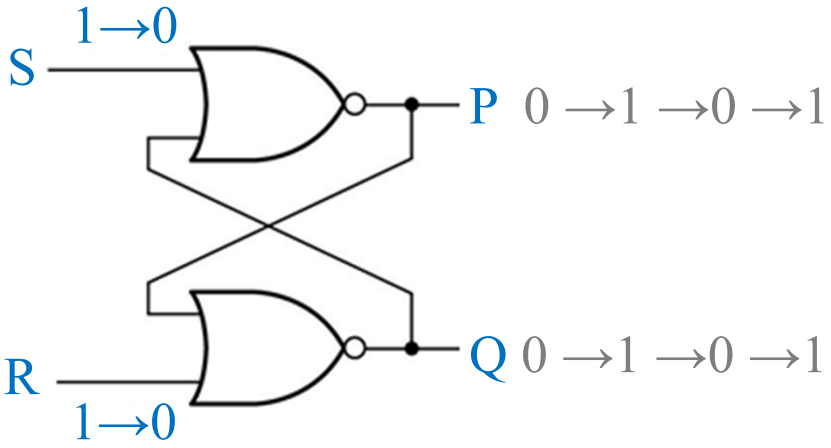
Symbol

Set-Reset Latch (SR Latch) (5/9)





Set-Reset Latch (SR Latch) (6/9)



if $S = R = 1 \rightarrow 0$ at the same time,

$\Rightarrow Q = P(Q')$

$= 0 \rightarrow 1 \rightarrow 0 \ldots$ (not allowed)

or $Q = 1$ first

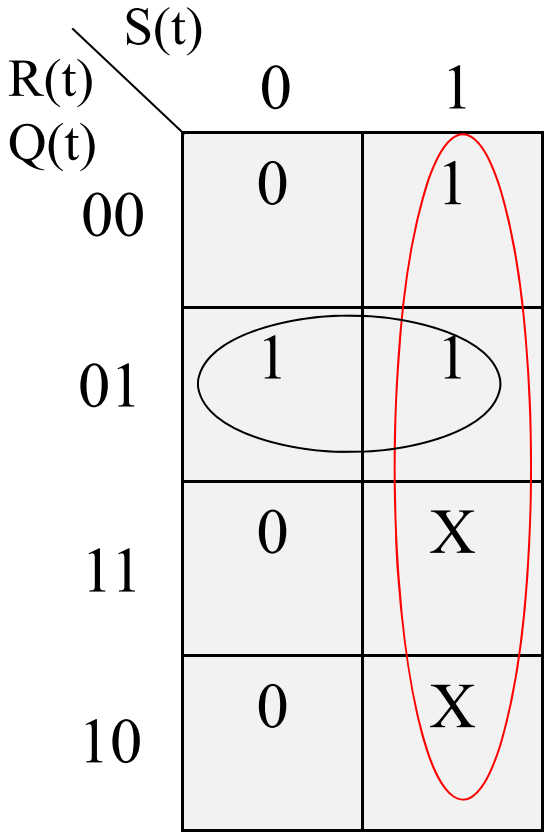
$Q' = 1$ first (undetermined)

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\varepsilon)$ $(= Q^+(t))$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	– } inputs not allowed
1	1	1	–

Set-Reset Latch (SR Latch) (7/9)

$$Q(t+\varepsilon) = S(t) + R'(t)Q(t) \text{ or}$$

$$\underbrace{Q^+ = S + R'Q}_{\text{characteristic equation}} \qquad (\text{when } SR = 0 \text{ or } SR \neq 11)$$



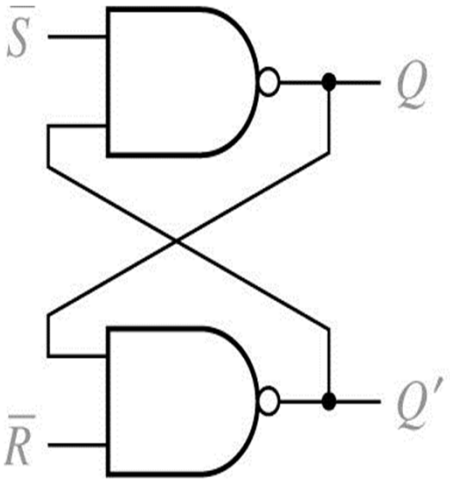
S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	–

Q_n : present state

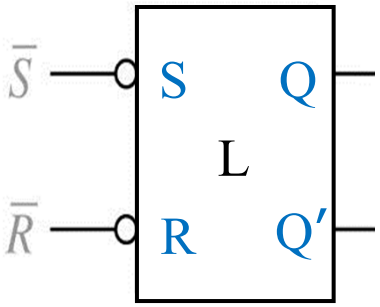
Q_{n+1} : next state

Set-Reset Latch (SR Latch) (8/9)

Alternative form using NAND gates



(a)



(b)

$\overline{S(t)}$	$\overline{R(t)}$	$Q(t)$	$Q(t+\varepsilon)$ $\left(=\mathrm{Q}^{+}(\mathrm{t})\right)$
1	1	0	0
1	1	1	1
1	0	0	0
1	0	1	0
0	1	0	1
0	1	1	1
0	0	0	– } inputs not allowed
0	0	1	– } inputs not allowed

$\overline{S}$	$\overline{R}$	Q_{n+1}
1	1	Q_n
1	0	0
0	1	1
0	0	–

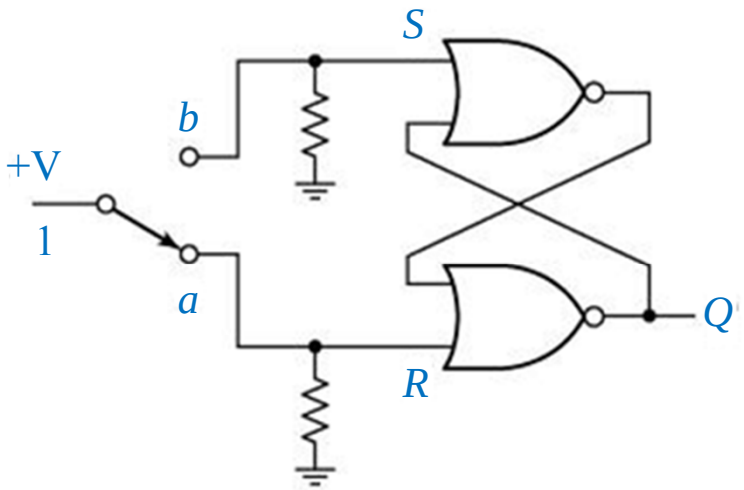
$\mathrm{Q_n}$: present state

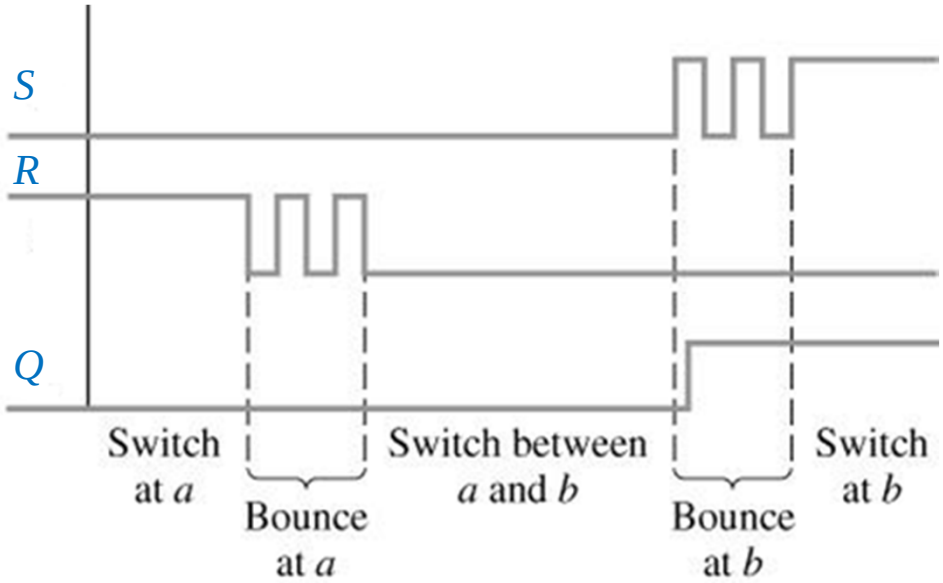
$\mathrm{Q_{n+1}}$: next state

Set-Reset Latch (SR Latch) (9/9)

Usage of SR latch

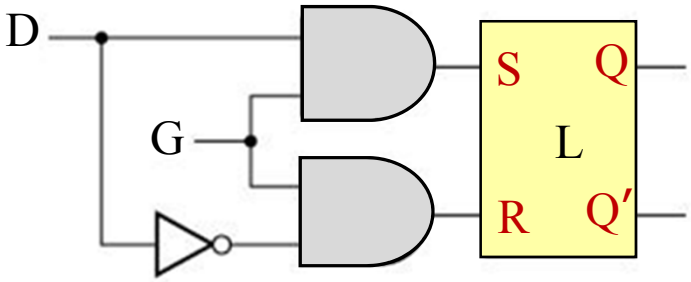
1. As a component in more complex latches and F/Fs
2. For debouncing switches



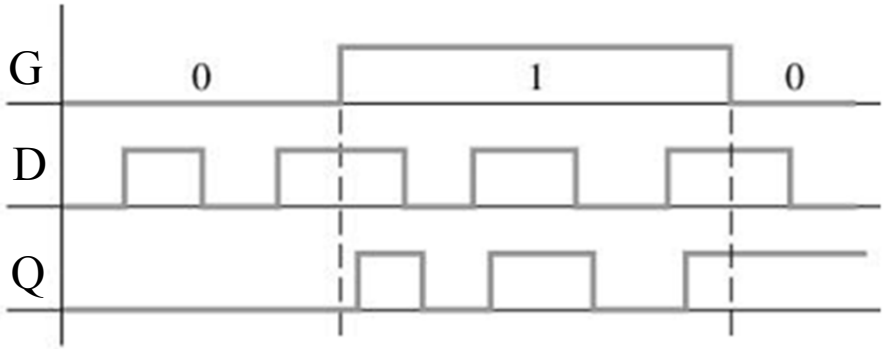


Gated D Latch

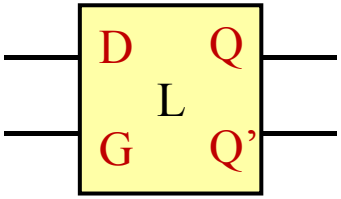
Transparent latch since G=1, Q = D



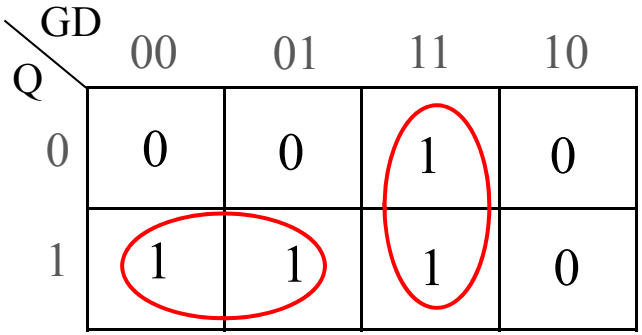
(a)



(b)



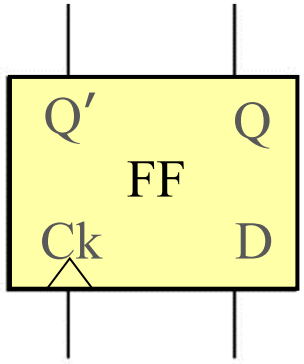
G	D	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



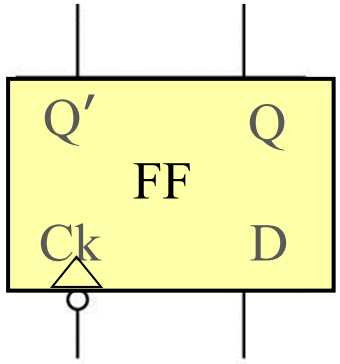
$$Q^+ = G'Q + GD$$

Edge-Triggered D Flip-Flop (1/5)

Similar to D latch, but changes only to clock edge



(a) Rising-edge trigger



(b) Falling-edge trigger

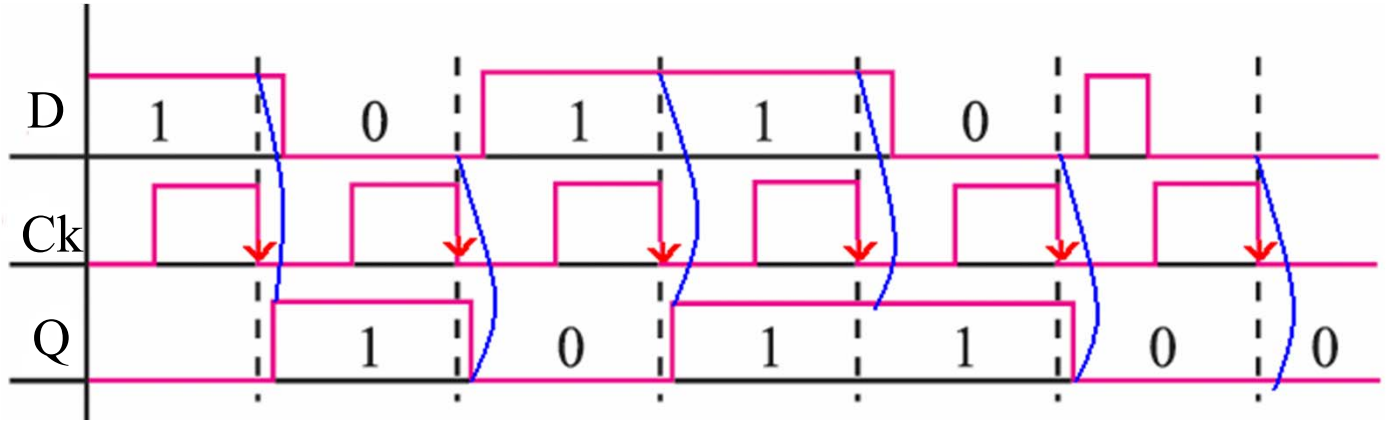
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

D	Q_n^+
0	0
1	1

$Q^+ = D$

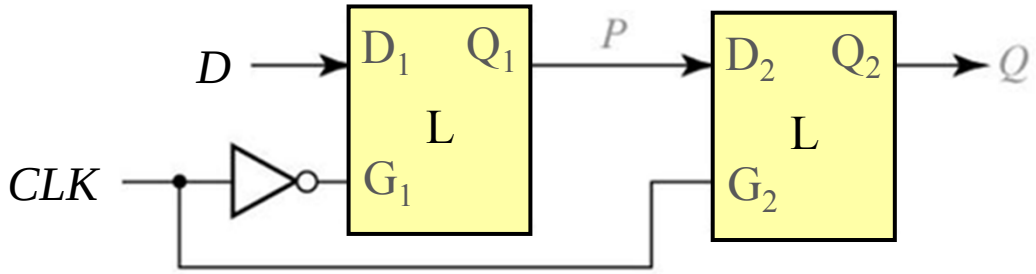
Edge-Triggered D Flip-Flop (2/5)

Timing diagram of falling edge triggered D F/F

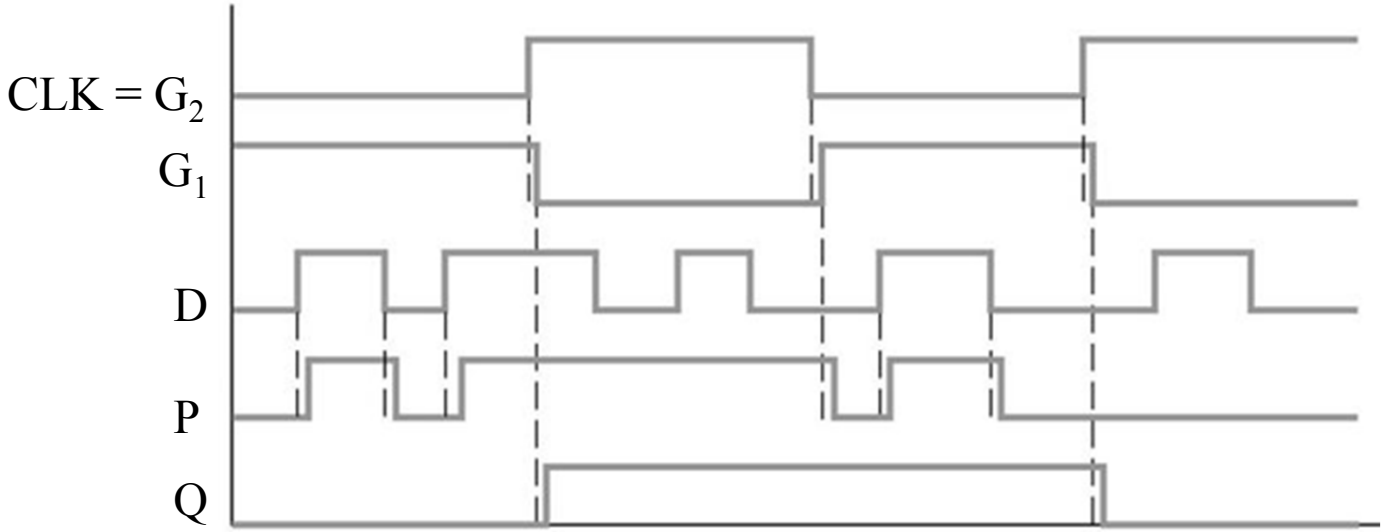


Edge-Triggered D Flip-Flop (3/5)

Timing diagram of rising edge triggered D F/F



(a) Construction from two gated D latches

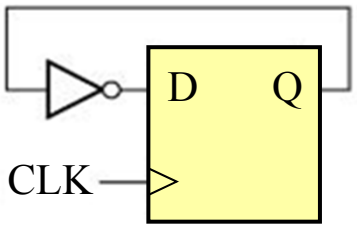


(b) Time analysis

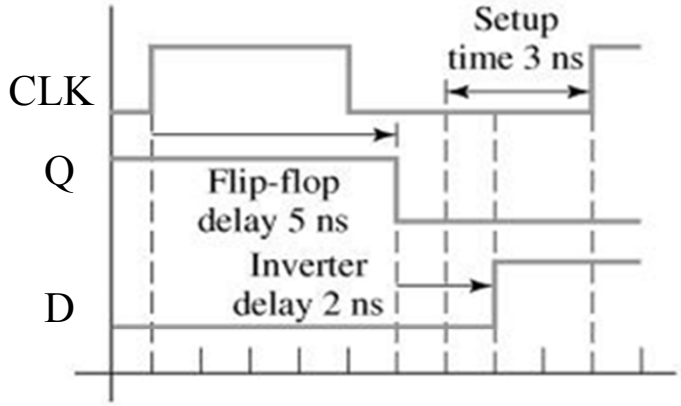
Edge-Triggered D Flip-Flop (4/5)

- Determine the minimum clock period
  - Minimum clock period
    =(total delay of gates) + (total delay of F/F)
- Example: suppose that
  - Propagation delay of the inverter = 2*ns*,
  - Propagation delay of the D F/F = 5*ns*,
  - Setup time of the D F/F = 3*ns*,
  - Determine the minimum clock period of the circuit

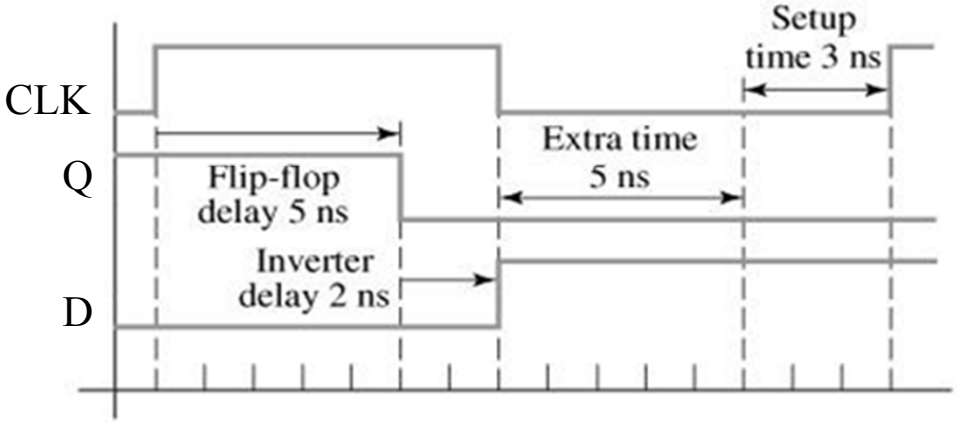
Edge-Triggered D Flip-Flop (5/5)



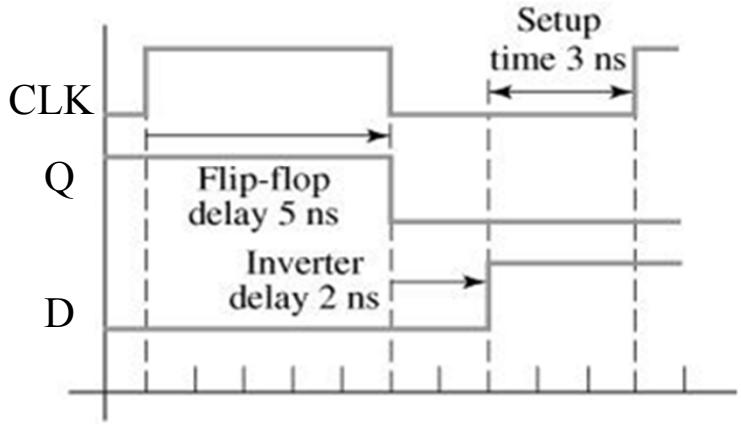
(a) Simple flip-flop circuit



(b) Setup time not satisfied



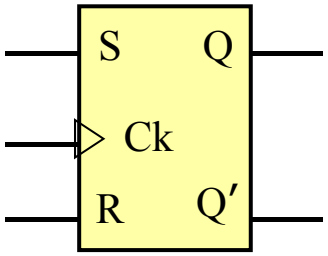
(c) Setup time satisfied



(d) Minimum clock period

S-R Flip-Flop (1/2)

Similar to SR latch, but has an extra clock input and changes only at clock edge



Operation summary:

S=R=0 no state change

S=1, R=0 set Q to 1 (after active Ck edge)

S=0, R=1 reset Q to 0 (after active Ck edge)

S=R=1 not allowed

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	–
1	1	1	–

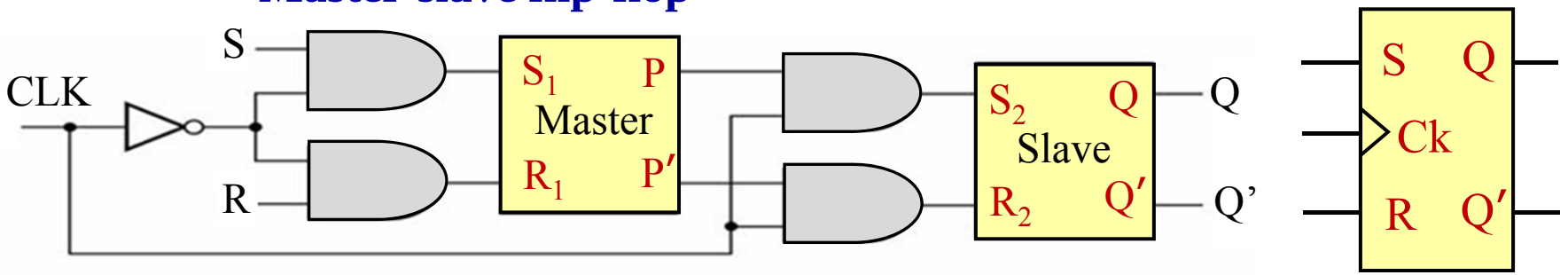
inputs NOT allowed

RQ \ S	0	1
00	0	1
01	1	1
11	0	X
10	0	X

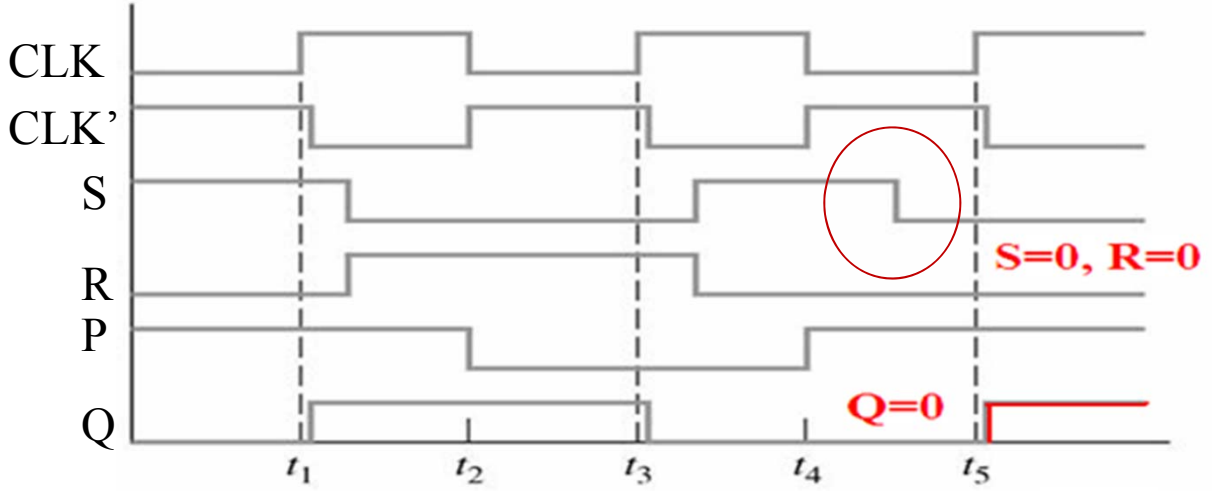
$$Q^+ = S + R'Q$$

S-R Flip-Flop (2/2)

- **Implementation of S-R Flip-Flop**
  - **Constructed from two S-R latches and gates**
  - **Master-slave flip-flop**



(a) Implementation with two latches



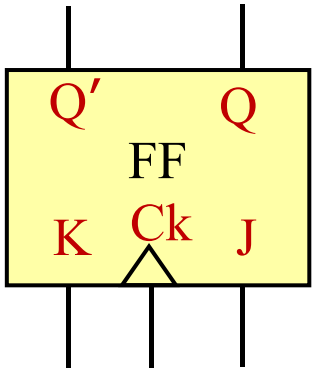
(b) Timing analysis

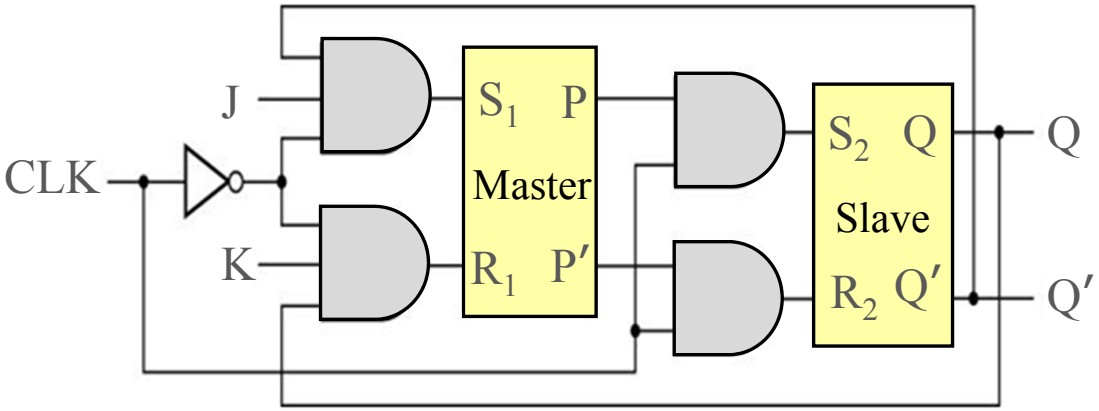
At t_5 , S=R=0, the state of Q should not change

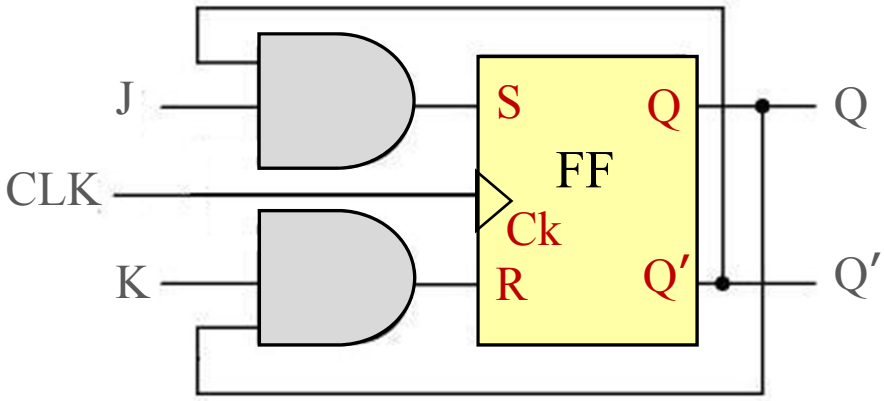
We can solve this problem if we only allow the S and R inputs to change while the clock is high

J-K Flip-Flop (1/3)

- **Implementation of J-K Flip-Flop**

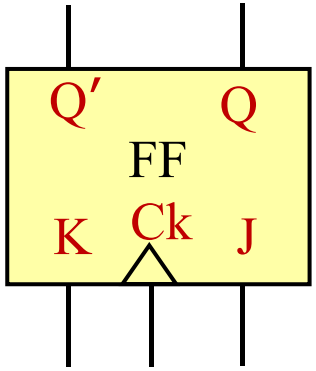






Q Changes on Rising Edge

J-K Flip-Flop (2/3)



J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q^+ = Q$

$Q^+ = 0$

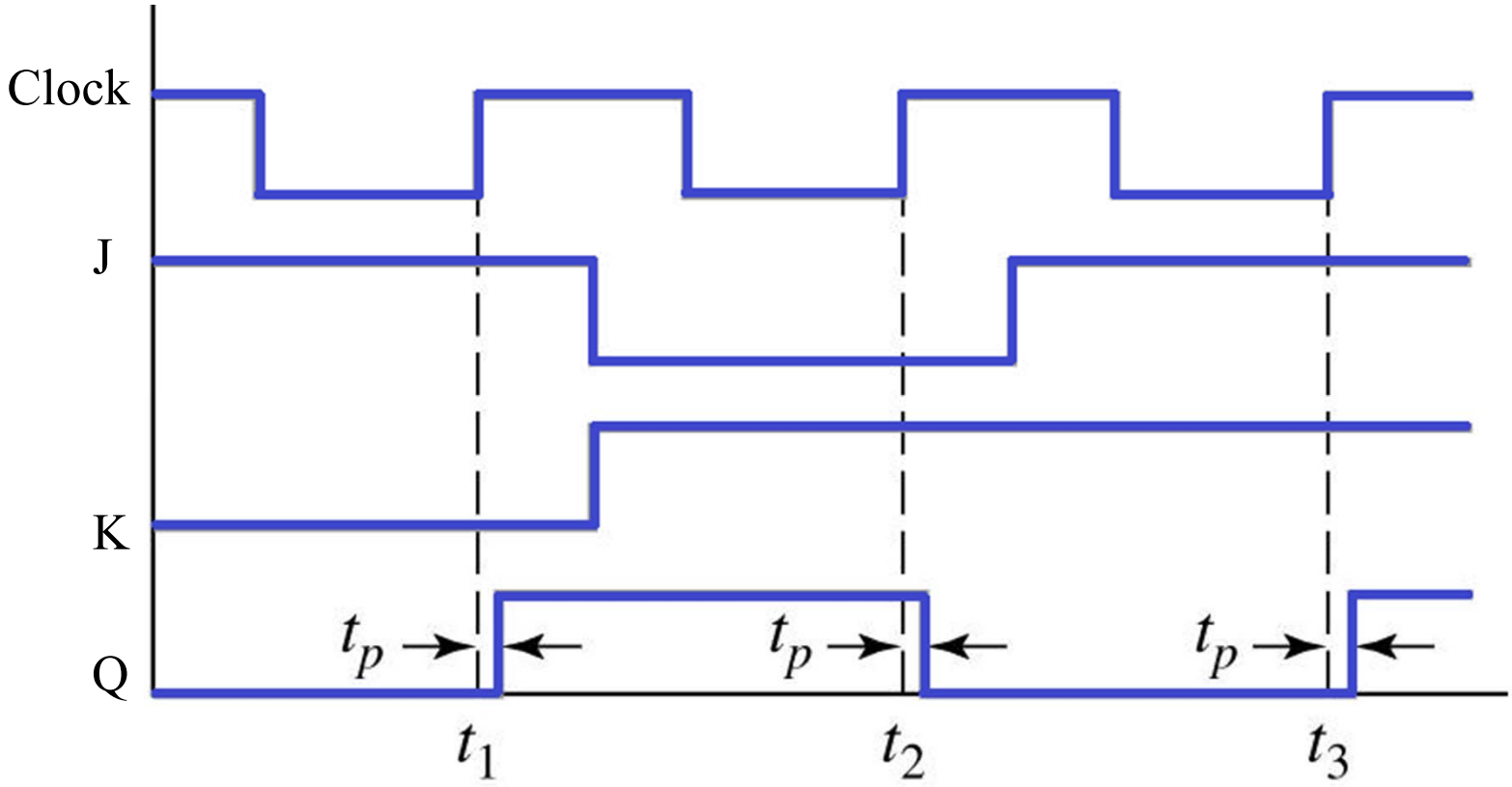
$Q^+ = 1$

$Q^+ = Q'$

$Q^+ = JQ'+K'Q$

Q \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

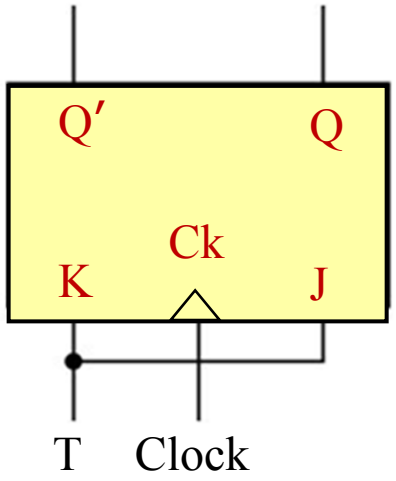
J-K Flip-Flop (3/3)

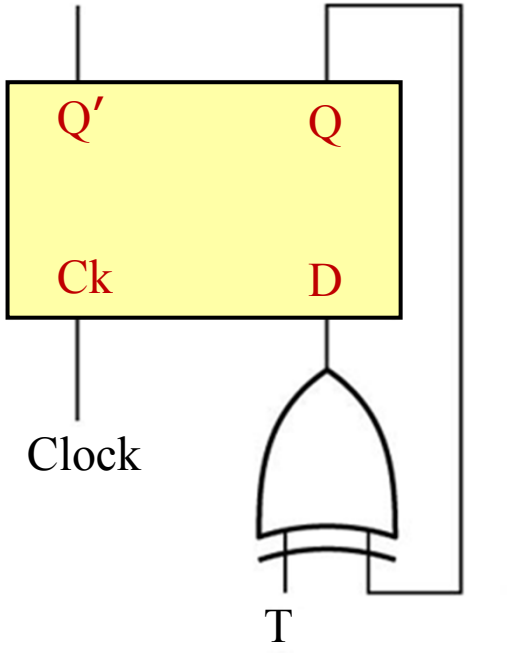


J-K flip-flop timing

T Flip-Flop (1/3)

- **Implementation of T (Toggle) Flip-Flop**





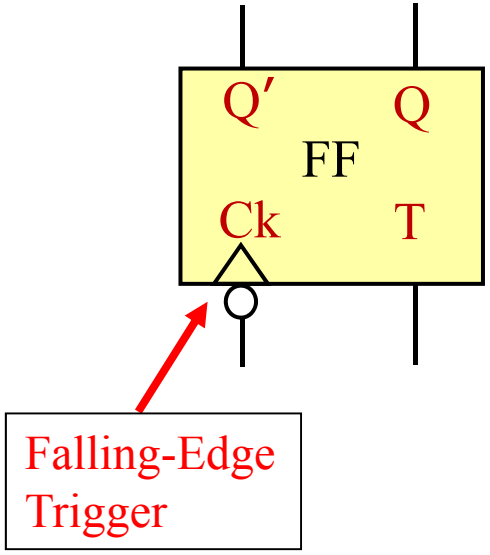
(a) Conversion of J-K to T

$$Q^+ = JQ' + K'Q = TQ' + T'Q$$
$$= Q \oplus T$$

(b) Conversion of D to T

$$Q^+ = Q \oplus T$$
$$= TQ' + T'Q$$

T Flip-Flop (2/3)

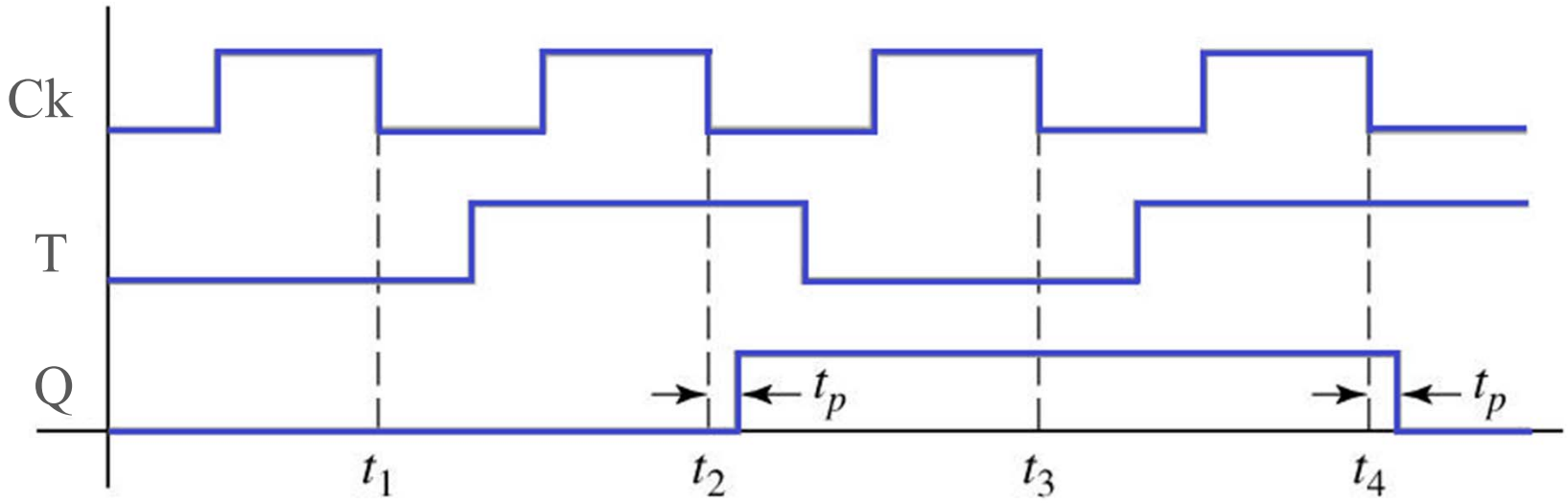


T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T'Q + TQ' = \mathrm{T} \oplus \mathrm{Q}$$

T Flip-Flop (3/3)

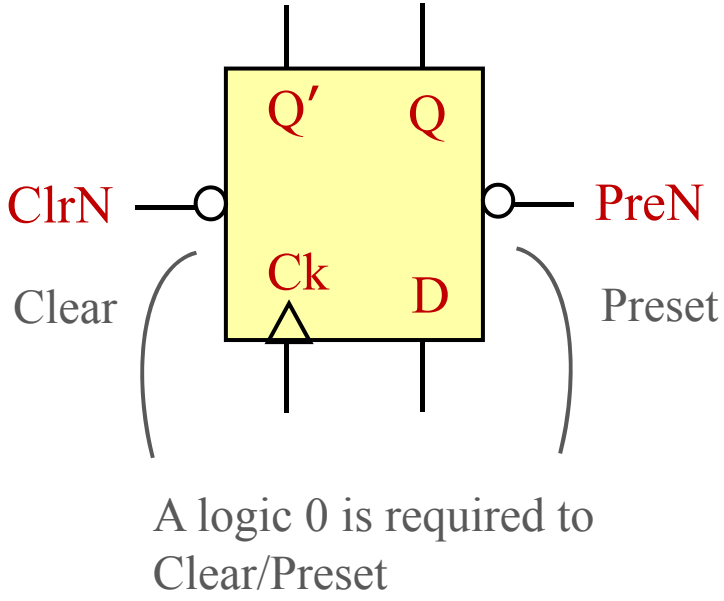
- **Timing diagram for T Flip-Flop**



Falling-Edge Trigger

Flip-Flops with Additional Inputs (1/4)

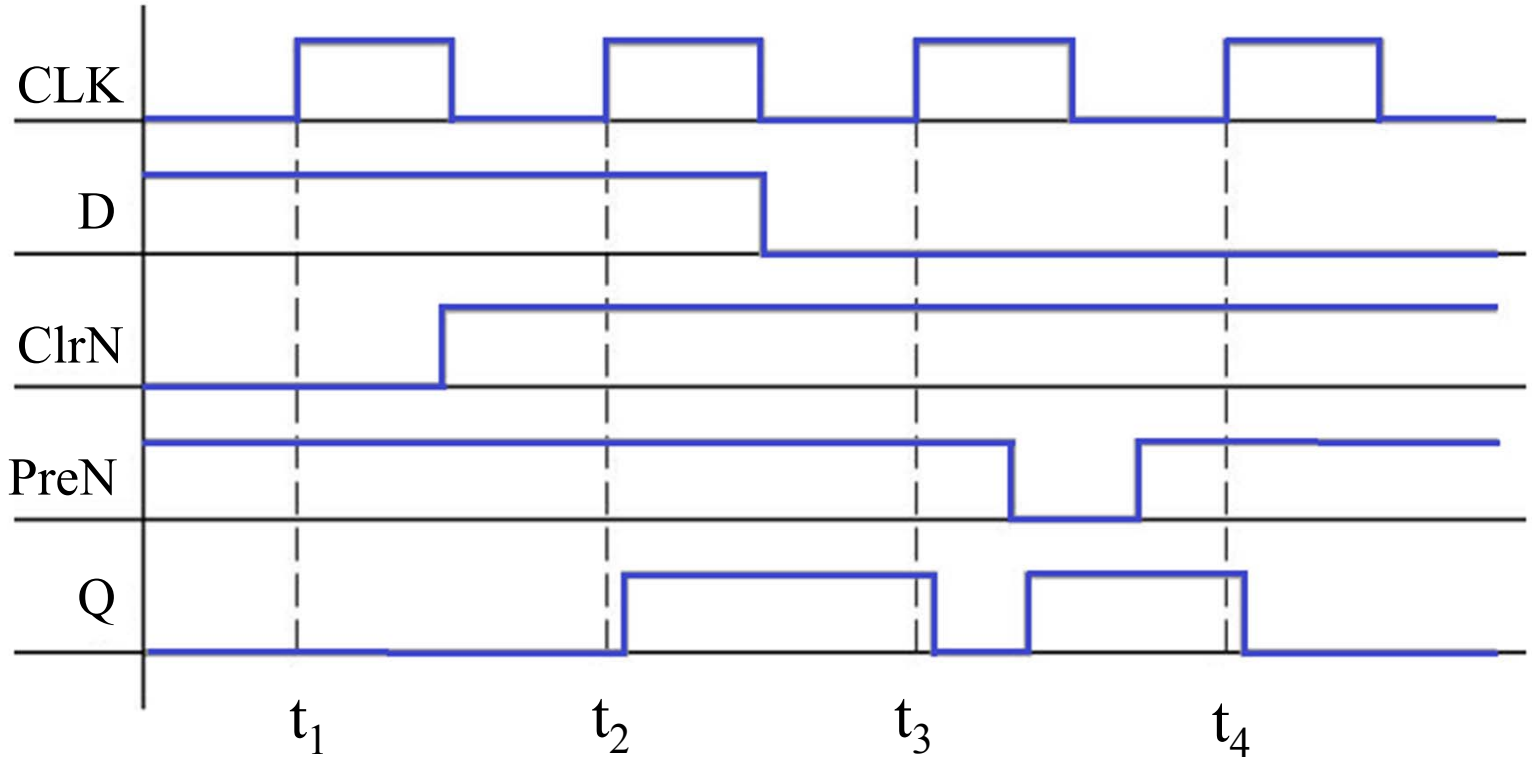
- **Flip-Flop with Clear and Preset Inputs**



Ck	D	*PreN*	*ClrN*	Q^+
×	×	0	0	(*not allowed*)
×	×	0	1	1
×	×	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1,↓	×	1	1	*Q*(*no change*)

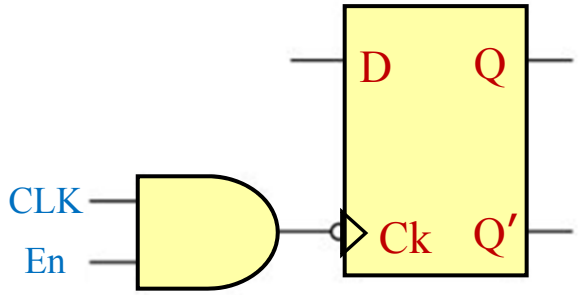
Flip-Flops with Additional Inputs (2/4)

- Timing diagram for rising-edge trigger D Flip-Flop with Clear and Preset



Flip-Flops with Additional Inputs (3/4)

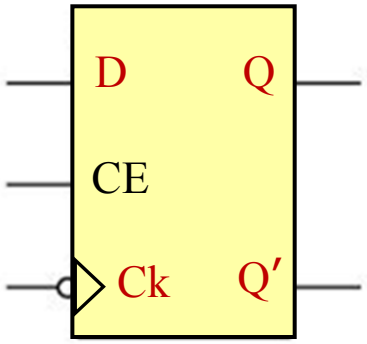
- Gating the Clock
  - Holding existing data even though the data input to the Flip-Flop is changing
  - Two potential problems:
    - Gate delays may cause the clock to arrive at some Flip-Flops at different times than at other Flip-Flops, resulting in loss of synchronization
    - If En changes at the wrong time, the Flip-Flop may trigger due to the change in En instead of due to the change in the clock, resulting in loss of synchronization



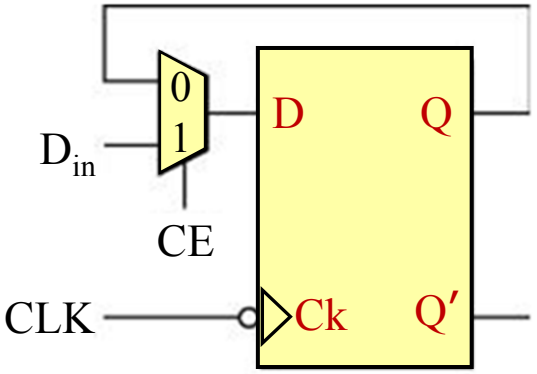
(a) Gating the clock

Flip-Flops with Additional Inputs (4/4)

- D Flip-Flop with Clock Enable (D-CE Flip-Flop)



(b) D-CE symbol



(c) Implementation

- CE=0, clock is disabled, $Q^+=Q$
- CE=1, the F/F acts like a normal D F/F, $Q^+=D$
- $Q^+=Q \cdot CE' + D \cdot CE$

Summary (1/3)

- The characteristic (next-state) equations for latches and F/Fs

$Q^+ = S + R'Q \; (SR = 0)$	(S-R Latch or Flip-Flop)
$Q^+ = GD + G'Q$	(Gated D Latch)
$Q^+ = D$	(D Flip-Flop)
$Q^+ = D \cdot CE + Q \cdot CE'$	(D-CE Flip-Flop)
$Q^+ = JQ' + K'Q$	(J-K Flip-Flop)
$Q^+ = T \oplus Q = TQ' + T'Q$	(T Flip-Flop)

Summary (2/3)

- Q represents an initial or present state of the Flip-Flop, and Q^+ represents the final or next state
  - The interpretation of Q^+
    - For latch

      Q+ represents the state of the latch a short time after one of the inputs changes
    - For Flip-Flop

      Q+ represents the state of the Flip-Flop a short time after the active clock edge

Summary (3/3)

- Flip-Flops constructed from S-R Flip-Flop