2018 Spring CS 210002 電路與電子學一 (Circuits and Electronics (I))

1.1: Semiconductor materials and properties

Device: Diode, BJT, FET

What is semiconductor ?

Conductor (metal)

Insulator

Free electrons
~$10^{22}/cm^3$
~$10^{0\sim1}/cm^3$
~$10^{10}/cm^3$

III	IV	V
B (硼)	C (碳)	
Al (鋁)	Si (矽)	P (磷)
Ga (鎵)	Ge (鍺)	As (砷)
	Sn (錫)	
	Pb (鉛)	

Insulator ⟶ Semi. ⟶ Conductor

Elemental semi : Si, Ge
Compound semi : GaAs (砷化鎵)

1.1.1: Intrinsic semiconductor

C: 2-4
Si: 2-8-4
Ge: 2-8-18-4
Sn: …
Pb: …

Valence electron (價電子)

Covalence bond (共價鍵)

Bandgap energy Eg :

1eV = 1.6×10^{-19} Joules
Electron ⟺ hole
電子 電洞
(e^-) (h^+)
e^- h^+ pair (電子電洞對)
n : 電子濃度 negative
p : 電洞濃度 positive

n = p = ni(T)

ni(T) (intrinsic carrier concentration)
$= BT^{3/2} e^{(-Eg/2kT)}$

Effect : 導電係數 ↑

For Si

$B = 5.23 \times 10^{15}\ cm^{-3}K^{-3/2}$
$k = 86 \times 10^{-6}$ eV /K (Boltzmann's Const)
T = 絕對溫度 K
Eg = 1.1 eV

$ni(T) = n = p = 1.5*10^{10} / cm^3$ at T=300K

V impurity : donate electron, n ↑↑
Donor (施體 or 施子)
Nd : donor impurity concentration

$$n \cong Nd >> ni$$

n-type semi.

Semi. has two current components

e^- flow
h^+ flow
} the same direction

Conductor has only one e^- flow

1.1.2: Extrinsic semiconductor

doping (摻雜)

why doping ?

Mass – Action law (質量作用定律)

$$n \times p = ni(T)^2$$

$$n >> p$$

impurities : { III : B
V : P, As

How ?

How many ?

e^- : majority carrier (多數載子)
h^+ : minority carrier (少數載子)

III impurity : accept electron, p ↑↑
Acceptor (受體 or 受子)
Na : acceptor impurity concentration

$$p \cong Na >> ni$$

p-type semi.

$$p >> n$$

e^- : minority carrier
h^+ : majority carrier

charge neutrality (電中性)

doping changes current components in semiconductor

1.1.3: Drift and diffusion current

Total current in semi.

= e^- current ＋ h^+ current

Two mechanisms: Drift and Diffusion

Drift current (e^- ＋ h^+)

$$Volt \rightarrow E \rightarrow F \rightarrow carrier\ moving(Vd)$$

$$Volt\uparrow \rightarrow E\uparrow \rightarrow F\uparrow \rightarrow Vd\uparrow \rightarrow I\uparrow$$

Drift velocity

= ohm's law

Mobility (移動率) μ

$Vd = \mu \bullet E \quad [\mu] = \left[\text{cm}/\text{s} \right] / \left[\text{V}/\text{cm} \right] = \frac{\text{cm}^2}{V \cdot s}$

$Vdn = -\mu_n \bullet E \quad$ for e^-, $\mu_n = 1350 \ \text{cm}^2/\text{V} \cdot s$

$Vdp = \mu_p \bullet E \quad$ for h^+, $\mu_p = 480 \ \text{cm}^2/\text{V} \cdot s$

$Jn = -qnV, \quad Vdn = -\mu_n \bullet E$

$Jn = -qn(-\mu_n \bullet E) = qn\mu_n \bullet E$

$[Jn] = \left[A/cm^2 \right] = \frac{col}{s \bullet cm^2}$

$Jp = qp(\mu_p \bullet E) = qp\mu_p \bullet E$

$J = Jn + Jp = qn\mu_n E + qp\mu_p E$

$= (qn\mu_n + qp\mu_p) \bullet E = \sigma \bullet E$

$\sigma(Conductivity) = \frac{J}{E} = qn\mu_n + qp\mu_p$

$[\sigma] = \frac{1}{\Omega \bullet \text{cm}}$

$R = \rho \bullet \frac{L}{A} \quad I = \frac{V}{R} \quad \rho \equiv$ resistivity

$J \bullet A = \frac{V}{R} = \frac{V}{\rho \bullet \frac{L}{A}} = E(1/\rho) \bullet A$

$J = E(\frac{1}{\rho}) = \sigma \bullet E$

$\Rightarrow \frac{1}{\rho} = \sigma \qquad \rho = \frac{1}{\sigma} = \frac{1}{qn\mu_n + qp\mu_p}$

$[\rho] = [\frac{1}{\sigma}] = \Omega \bullet cm$

Impurity scattering

$T \uparrow \qquad \mu \uparrow$

Lattice scattering

$T \uparrow \qquad \mu \downarrow$

Intrinsic semi. $\sigma = qn_i(\mu_n + \mu_p)$

$T\uparrow \quad n_i\uparrow \quad \mu\downarrow \Rightarrow \sigma\uparrow$

n-type semi. $\sigma = q\,n\mu_n = q\,N_d\,\mu$

$T\uparrow \quad \sigma\downarrow$

p-type semi. $\sigma = q\,p\mu_p = q\,N_a\,\mu$

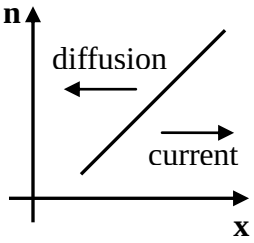
$T\uparrow \quad \sigma\downarrow$

Conductor $T\uparrow \quad \sigma\downarrow$

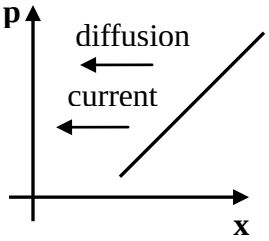
Diffusion current does not exist in conductor

Why diffusion?

Probability



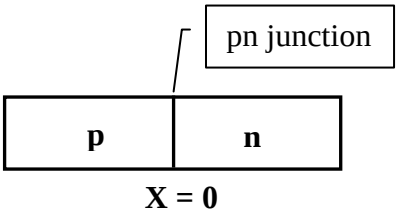
電子

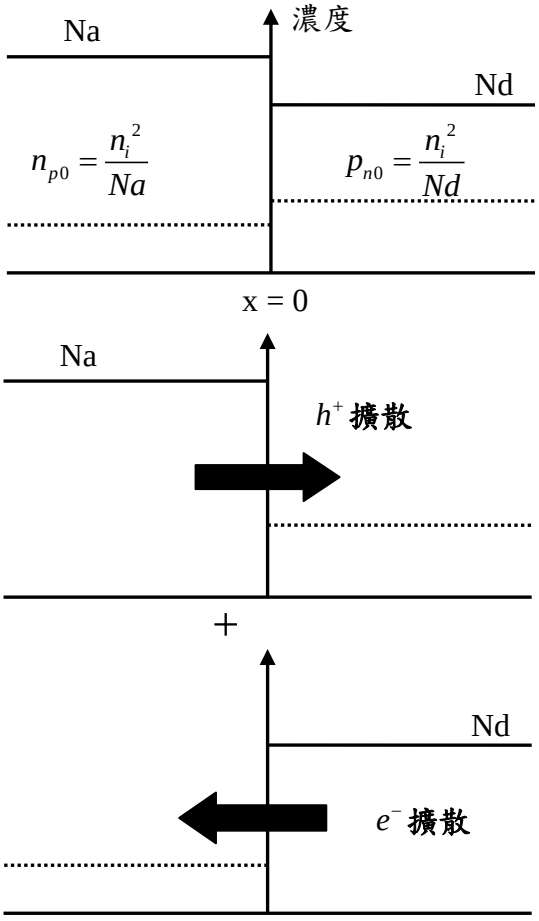


電洞

1.2: The PN junction

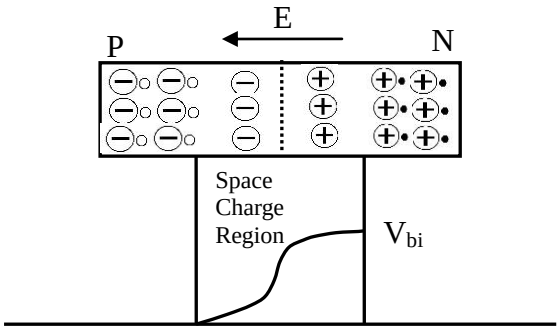
1.2.1: The equilibrium pn junction
(open circuit pn junction)





整體擴散電流向右

No current !!



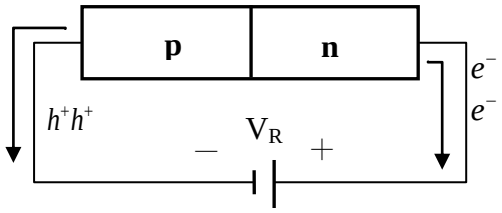
space-charge region or depletion region
(空間電荷區)　　(空乏區)

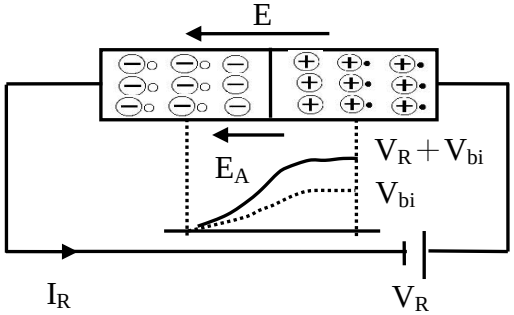
Built-in potential barrier (內建位障)

$= V_{bi} = V_T \ln(\frac{NaNd}{n_i^2})$

$V_T = KT/q$ (Thermal voltage) $= \frac{T}{11600}$

1.2.2 Reverse-biased pn junction

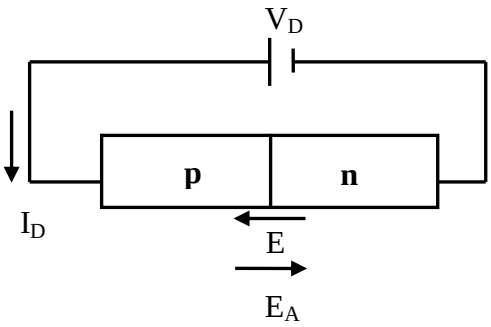




I_R=0

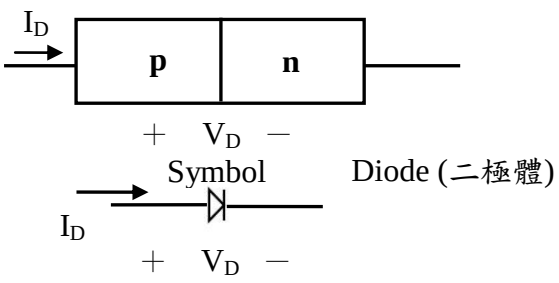
Reverse-bias saturation current I_s

1.2.3: Forward-biased pn junction



$I_D \neq 0$

1.2.4: Ideal current-voltage relationship



$$I_D = I_s(e^{V_D/nV_T} - 1)$$

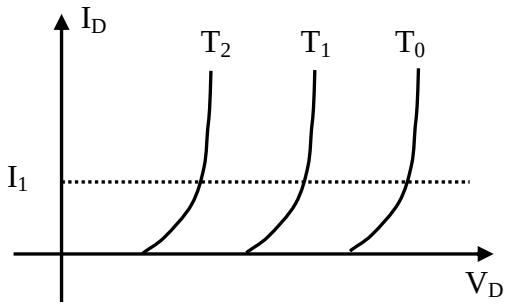
I_s : reverse-bias saturation current or scale current $\cong (10^{-15} \sim 10^{-9})$

n : ideality factor (1 or 2)

V_T : thermal voltage (熱電壓)

Cut-in voltage (切入電壓)

$V_D \Rightarrow -2mv/^oC$



T_2 T_1 T_0

breakdown (崩潰)

Avalanche breakdown (纍增崩潰)

Diode : 電壓控制開關

ON : 大電流 (外部電路決定)

OFF : 微小電流 = $-I_s$

Called 整流器 (rectifier)

$$I_s(t_2) = I_s(t_1) \times 2^{\frac{t_2 - t_1}{10}}$$

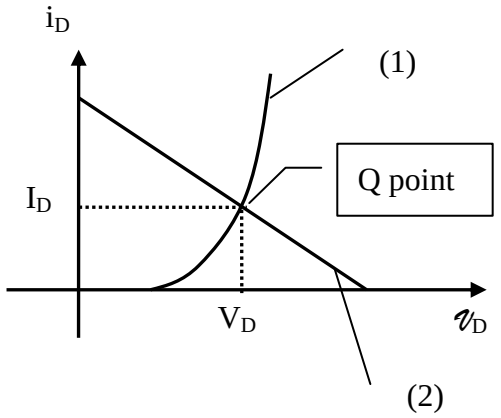
Zener breakdown (齊納崩潰)

$$I_D = I_S(e^{V_D/nV_T} - 1) \quad \text{---------- } (1)$$

$$V_{DD} = I_D \times \mathrm{R} + \mathrm{V_D} \quad \text{---------- } (2)$$

solve V_D? I_D?

1. Graphical analysis technique (圖解法)



zener : T↑, breakdown voltage↓

avalanche : T↑, breakdown voltage↑

PIV: (peak inverse voltage)

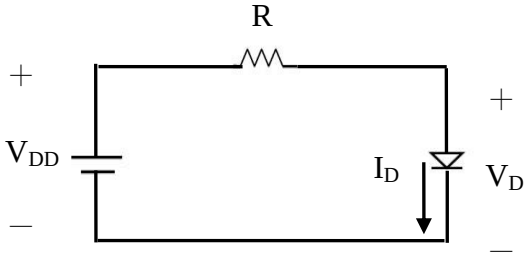
Zener diode : 工作於 breakdown region

1.3: Diodes circuit, DC analysis and models

DC 直流

AC 交流

Model



2. Iteration analysis (疊代法)

assume $V_D = 0.7V$

by (2) $I_D = \dfrac{V_{DD} - V_D}{R}$ ---------- (3)

by (1) $V_D = nV_T \ln(\dfrac{I_D}{I_S})$ ---------- (4)

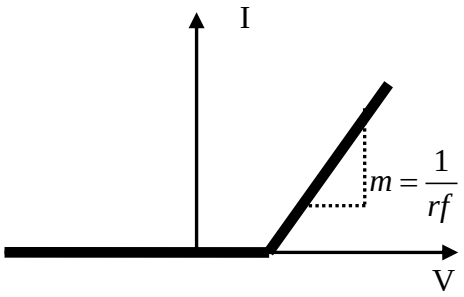
$V_D = 0.7$ 帶入(3)，求出 I_D

此 I_D 再代入(4)，求出 V_D (if 與 0.7 不符)

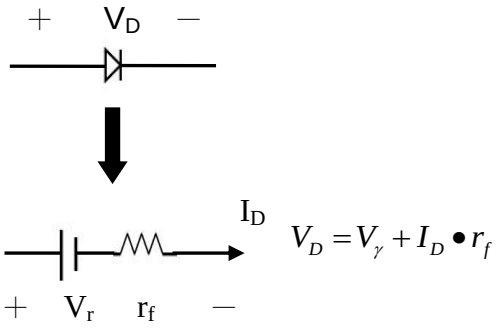
再代入(3)…...直到 V_D fixed.

物理意義

b. battery-plus-resistance model



Forward



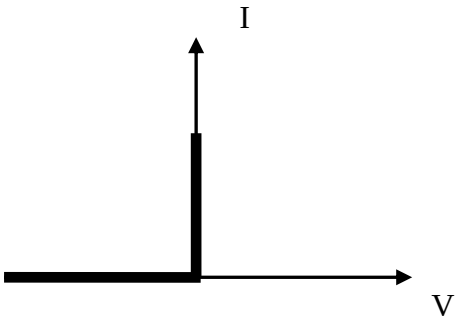
3. SPICE

   Tool supports

4. Approximation (近似法)

   Piecewise linear model, easy and fast

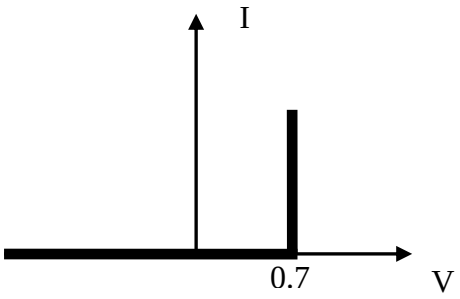
a. ideal diode model



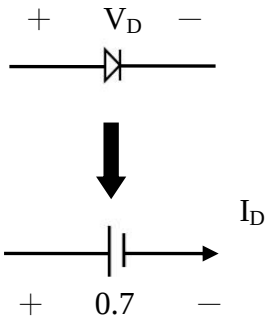
Forward $V_D = 0 \quad I_D > 0 \quad (short)$
Reverse $V_D < 0 \quad I_D = 0 \quad (open)$

Reverse (open)

c. constant-voltage drop model



Forward



Reverse (open)

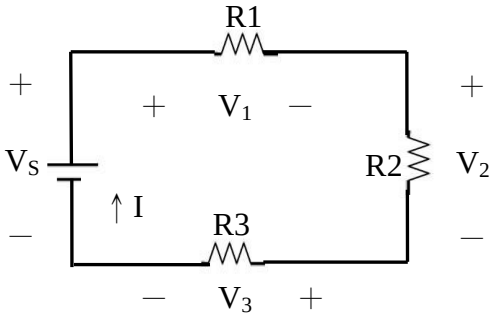
Tradeoff

基本電路理論

Kirchhoff's Voltage Law (KVL)

電壓昇 = 電壓降

迴路電壓和為 0



Conservation of Energy

$$IV_S - IV_1 - IV_2 - IV_3 = 0, I \neq 0$$

$$V_S - V_1 - V_2 - V_3 = 0$$

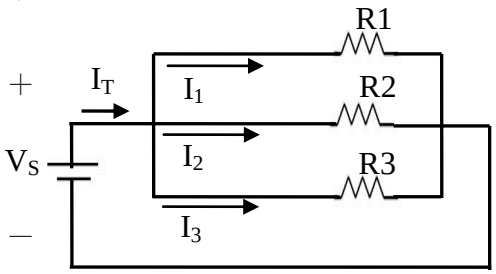
$$V_S = V_1 + V_2 + V_3$$

Resistors in series

Kirchhoff's Current Law (KCL)

流進 = 流出

節點電流和 = 0

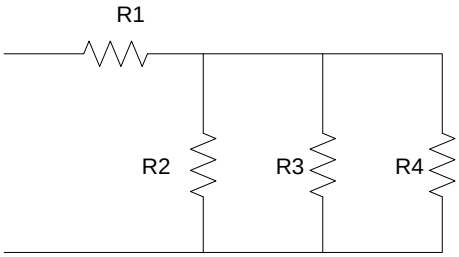


$$I_T - I_1 - I_2 - I_3 = 0$$

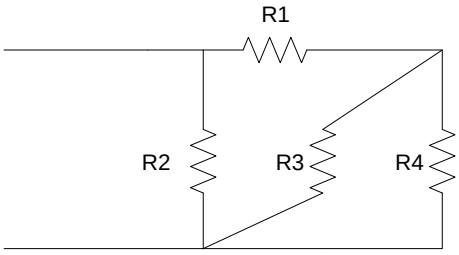
$$I_T = I_1 + I_2 + I_3$$

Resistors in parallel

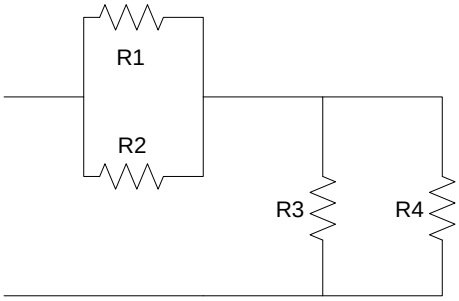
串並聯等效電路



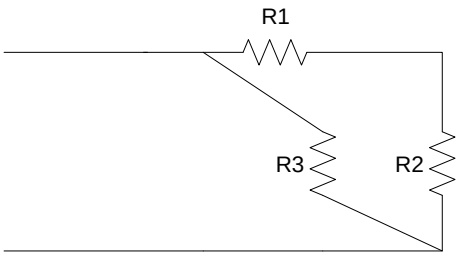
$$R = R_1 + (R_2 \,/\!/\, R_3 \,/\!/\, R_4)$$



$$R = R_2 \;/\!/\; (R_1 + R_3 /\!/ R_4)$$

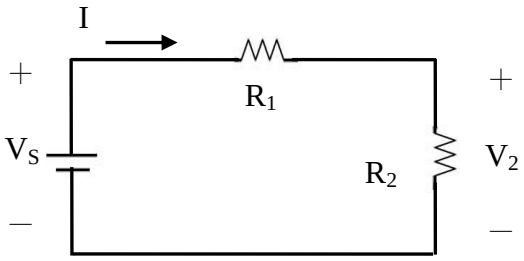


$$R = (R_1 \;/\!/ R_2) + (R_3 /\!/ R_4)$$



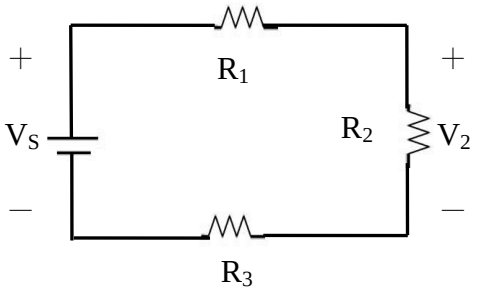
$$R = R_3 \;/\!/\; (R_1 + R_2)$$

分壓定律



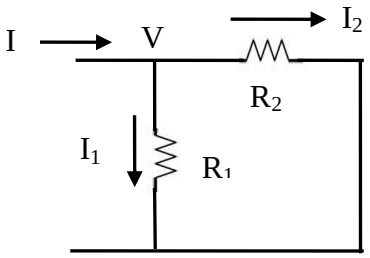
$$I = \frac{V_S}{R_1 + R_2} \quad (Ohm's\ law)$$

$$V_2 = I \bullet R_2 = \frac{V_S}{R_1 + R_2} \bullet R_2 = V_S \bullet \frac{R_2}{R_1 + R_2}$$



$$V_2 = V_S \bullet \frac{R_2}{R_1 + R_2 + R_3}$$

分流定律



$$I_1 = \frac{V}{R_1} \qquad I_2 = \frac{V}{R_2}$$

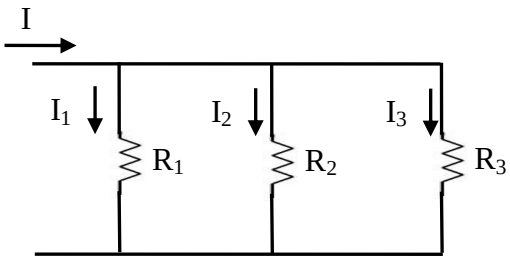
$$V = I_1 \bullet R_1 = I_2 \bullet R_2 \qquad I_1 = \frac{R_2}{R_1} \bullet I_2$$

$$I = I_1 + I_2 = \frac{R_2}{R_1} \bullet I_2 + I_2$$

$$= (\frac{R_2 + R_1}{R_1}) \bullet I_2$$

$$I_2 = \frac{R_1}{R_1 + R_2} \bullet I$$

$$I_1 = \frac{R_2}{R_1 + R_2} \bullet I$$



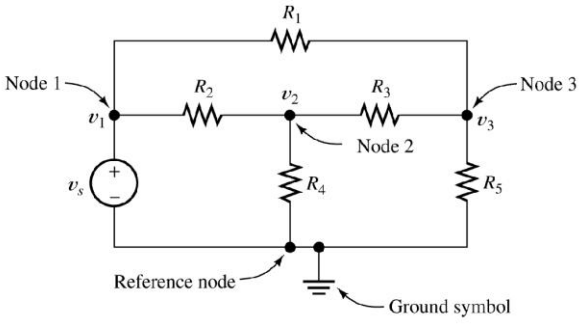
$$I_1 = \frac{R_2 /\!/ R_3}{R_1 + (R_2 /\!/ R_3)} \bullet I$$

Where $R_2 /\!/ R_3 = \dfrac{1}{\frac{1}{R_2} + \frac{1}{R_3}} = \dfrac{R_2 \bullet R_3}{R_2 + R_3}$

Node Analysis (節點分析法)

Steps : 1 決定參考點(及電流方向)
2 指定節點電壓
3 列出每個節點的 KCL 方程式
4 解聯立方程式

Ex :

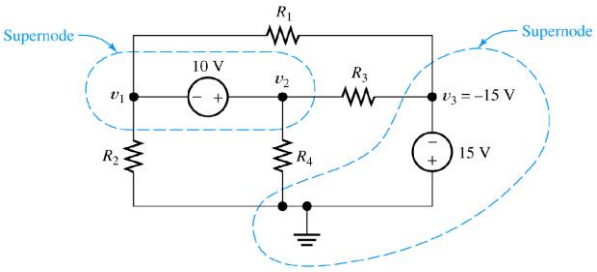


$$\frac{V_1 - V_2}{R_2} + \frac{V_3 - V_2}{R_3} - \frac{V_2}{R_4} = 0$$

$$\frac{V_1 - V_3}{R_1} = \frac{V_3 - V_2}{R_3} + \frac{V_3}{R_5}$$

$V_1 = V_s$ (可少一個變數)

Ex :



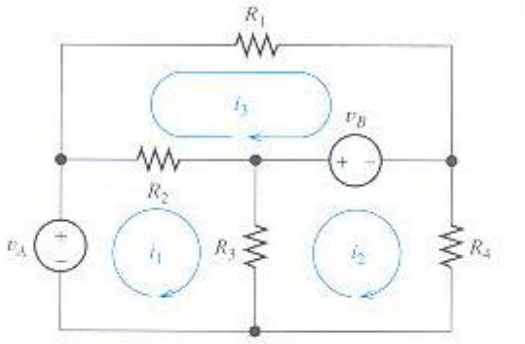
$$V_1 + 10 = V_2$$

$$\frac{V_1}{R_2} + \frac{V_2}{R_4} + \frac{V_1 - (-15)}{R_1} + \frac{V_2 - (-15)}{R_3} = 0$$

Mesh Analysis (網目分析法)

Steps : 1 決定網目電流方向
2 指定網目電流
3 列出每個網目的 KVL 方程式
4 解聯立方程式

Ex :

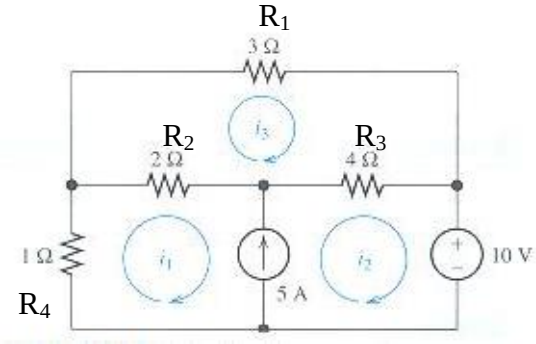


$$V_A = R_2(i_1 - i_3) + R_3(i_1 - i_2)$$

$$V_B = R_3(i_1 - i_2) - R_4 i_2$$

$$V_B = R_2(i_3 - i_1) + R_1 i_3$$

Ex :



$$10 = R_3(i_3 - i_2) + R_2(i_3 - i_1) + R_4(-i_1)$$

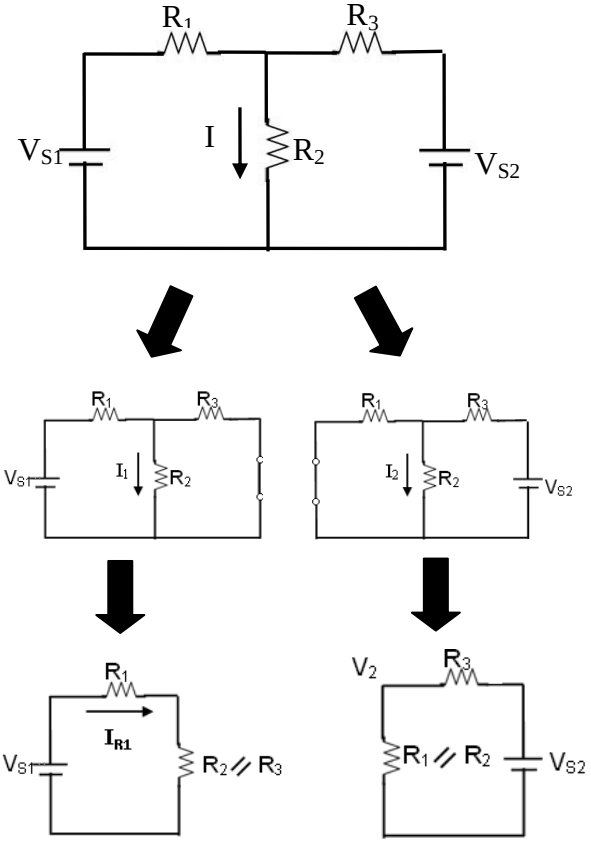
$$R_1 i_3 + R_3(i_3 - i_2) + R_2(i_3 - i_1) = 0$$

$$i_2 - i_1 = 5$$

Superposition Theorem (重疊定理)
欲處理電路中有多個電壓源或電流源時

Steps : 1 一次考慮一個電源的作用
"弄死"其他電源
V ⟶ short
I ⟶ open
2 解電路
3 將結果加起來

Ex :



$$I_{R1} = \frac{V_{S1}}{R_1 + (R_2 /\!/ R_3)}$$

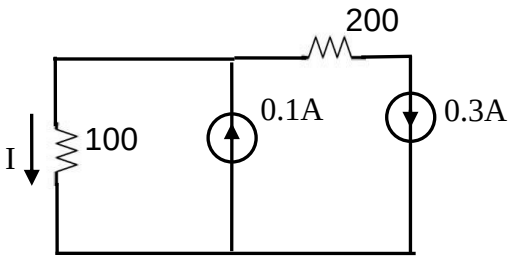
$$I_1 = I_{R1} \bullet \frac{R_3}{R_2 + R_3} \quad \text{(by 分流)}$$

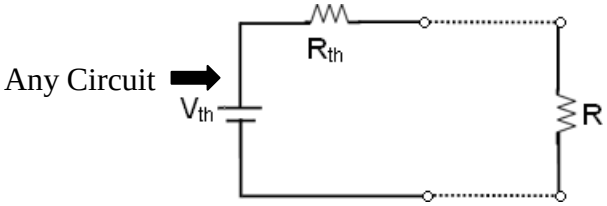
$$V_2 = V_{S2} \bullet \frac{R_1 /\!/ R_2}{(R_1 /\!/ R_2) + R_3} \quad \text{(by 分壓)}$$

$$I_2 = \frac{V_2}{R_2}$$

$$I = I_1 + I_2$$

Ex :



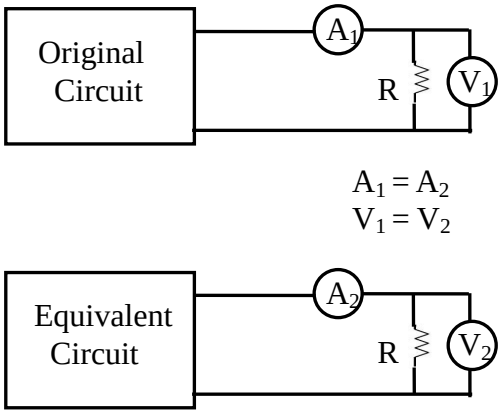


V_{th} : open circuit voltage
R_{th} : terminal resistance
(弄死電源)

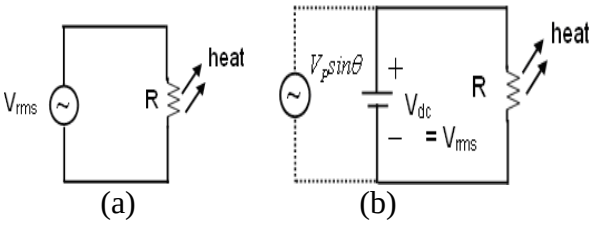
I = −0.2 A

Thevenin's Theorem (戴維寧定理)

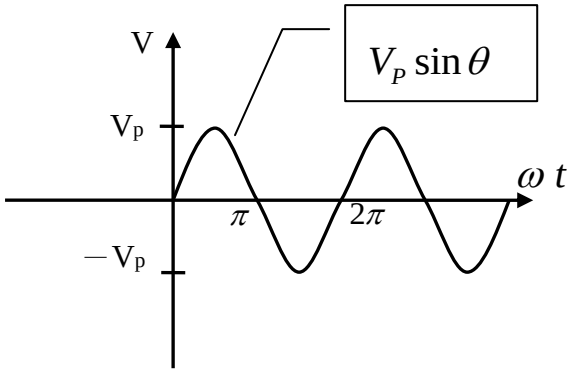
Terminal Equivalence:



Root Mean Square (RMS) value
(均方根值) or Effective value (有效值)
≡ The rms value of a sine wave is equal to the DC voltage that produces the same amount of heat as the sinusoidal voltage



Same amount of heat as in (a)



2.1: Rectifier circuit (整流電路)

V_P : *peak value*

V_{P-P} : *peak to peak value*

$V_{avg} = 0$

$V_P = \sqrt{2}\ V_{rms}$

$V_P \sin\theta = V_P \sin\omega t = V_P \sin(2\pi f)t$

ω: *angular frequency* $= 2\pi f$
(角頻率)

f : *Hertz* ($1/S$) 頻率

T : 週期 (s)

$f = \frac{1}{T}$

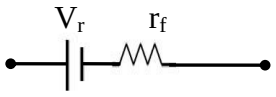
Half-wave 半波
Full-wave 全波

Input : 交流(AC)訊號 (極性不固定)
Output : 直流(DC)訊號 (極性固定)

Diode “單向導通”

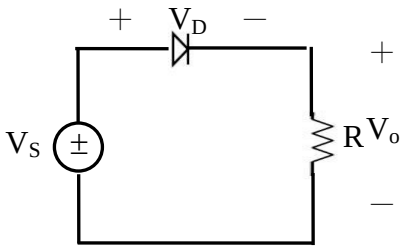
Diode model

Forward ON

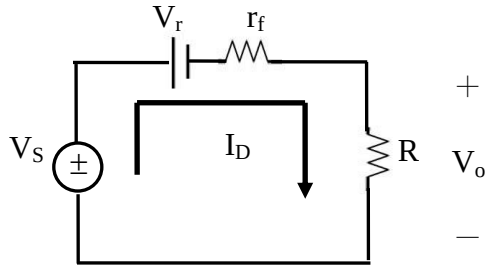


Reverse OFF

2.1.1: Half-wave rectifier (半波整流電路)



Forward $(V_S \geq V_r)$



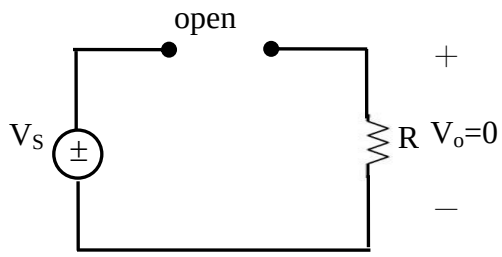
$$I_D = \frac{V_S - V_r}{r_f + R}$$

$$V_o = I_D \bullet R = (V_S - V_r)\frac{R}{r_f + R}$$

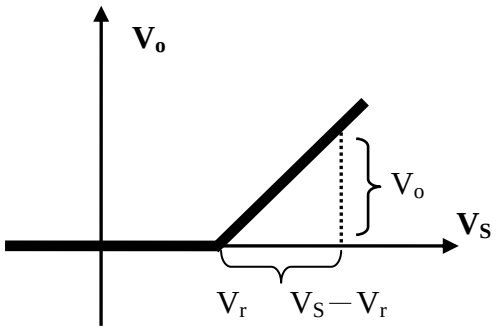
if $r_f = 0$, $V_o = V_S - V_r$

if $r_f = 0$, $V_r = 0$, $V_o = V_S$

Reverse $(V_S < V_r)$



Voltage Transfer Characteristic (VTC)
(電壓轉換特性曲線)

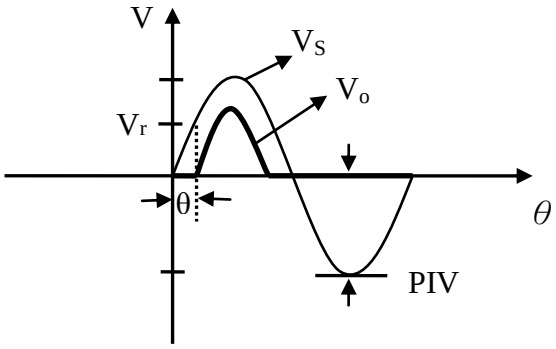


$$\frac{V_o}{V_S - V_r} = \frac{R}{r_f + R} = m$$

$m = 1$ if $r_f << R$

or $r_f = 0$

Vo waveform with Vs



$V_r = V_P \sin\theta$, $\theta = \sin^{-1}(\frac{V_r}{V_P}) \equiv cut-in\ angle$

(切入角)

V_D waveform with Vs

PIV = V_P

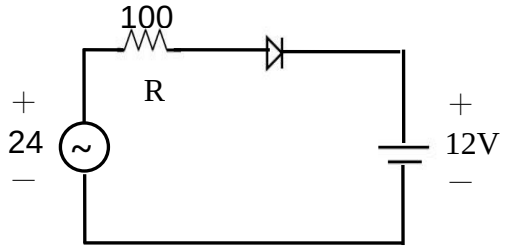
Half-wave rectifier:

1.不是 t=0 即有 V_o (cut-in angle)

2. peak value 不到 V_P

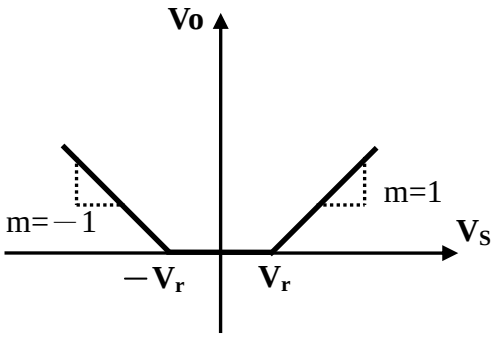
3. on state 不足 half period

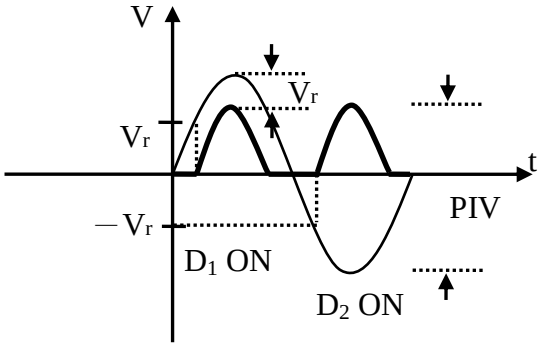
Ex:



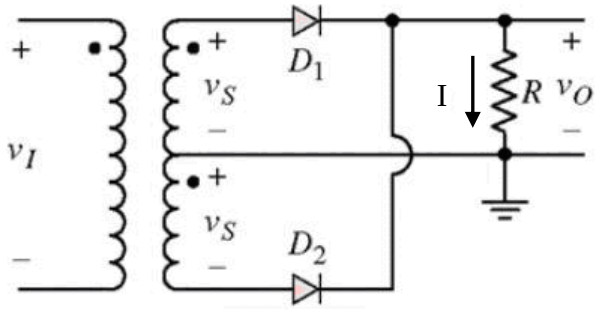
$V_r = 0.6V$ $r_f = 0$

VTC





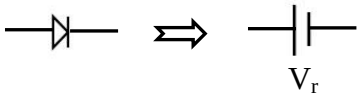
2.1.2: Full-wave rectifier (全波)



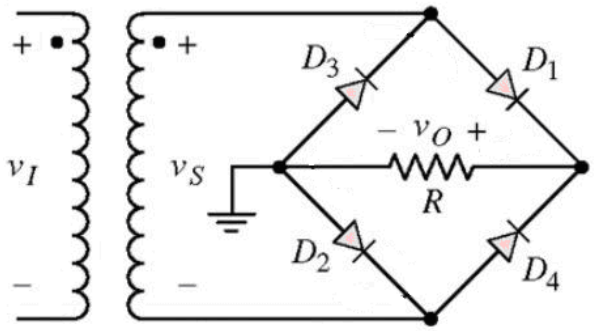
Overhead

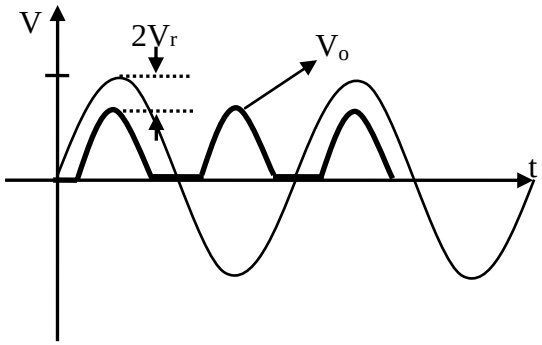
1. 線圈 2 倍，Diode 多一個
2. PIV = $2V_P - V_r$ ≒ 半波整流的 2 倍

Diode model



Bridge rectifier (橋式)

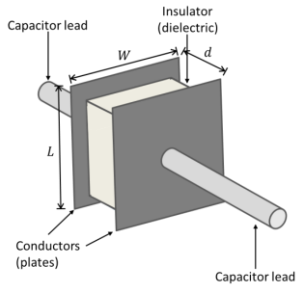




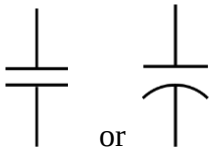
PIV = $V_P - V_r$

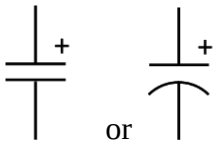
Ex:
V_I = 120 V (rms), given V_r = 0.7
desired V_o = 9 V (peak)
find $\frac{N_1}{N_2}$ & *PIV* in both Full-wave rectifiers

Capacitance (電容)
Capacitor (電容器)

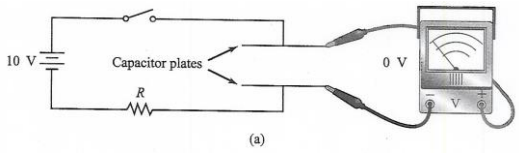


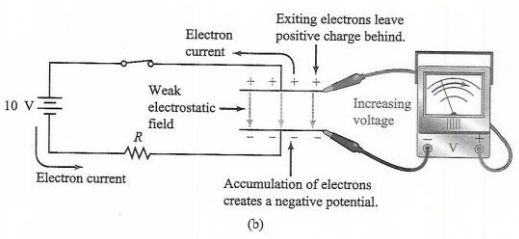
Symbol

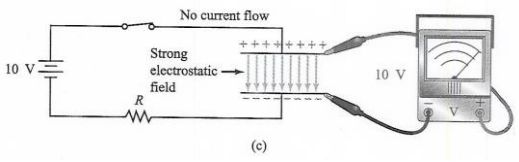
無極性電容  or

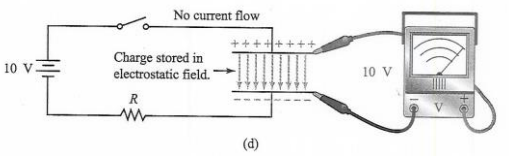
有極性電容  or

Charging process

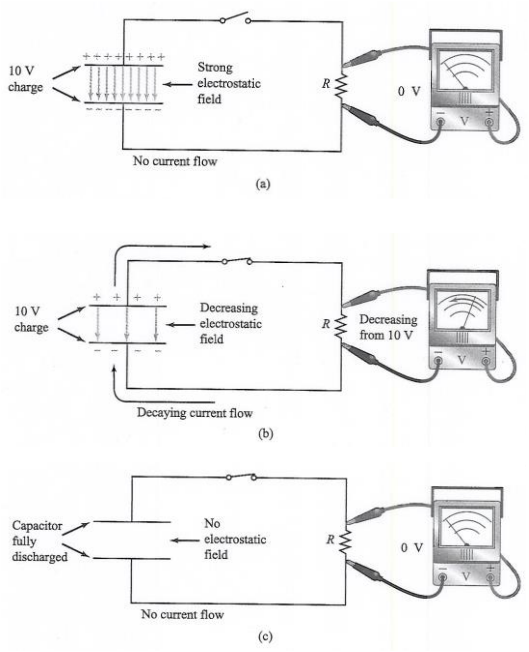








Discharging process



Capacitance computation for parallel-plate capacitors

$Area\ A = W \times L$

$$C = \frac{\epsilon A}{d}$$

Unit: Farad (法拉) = Coulomb/volt

ϵ is the dielectric constant of the material (permittivity 介電常數)

$\epsilon = \epsilon_r \epsilon_0$

$\epsilon_0 \cong 8.85 \times 10^{-12}$ F/m for vacuum

ϵ_r is the relative dielectric constant

Materials	ϵ_r
Air	1.0
Mica	7.0
Quartz	4.3
Water	78.5

Ex:

Compute the capacitance of a parallel-plate capacitor having rectangular plates 10 cm by 20 cm separated by a distance of 0.1 mm. The dielectric is air.

Sol:

$$C = \frac{\epsilon A}{d} = \frac{8.85 \times 10^{-12} \times 0.02}{10^{-4}} = 1770 \times 10^{-12}\ \text{F}$$

microfarads =

picofarads =

The voltage-current relationship

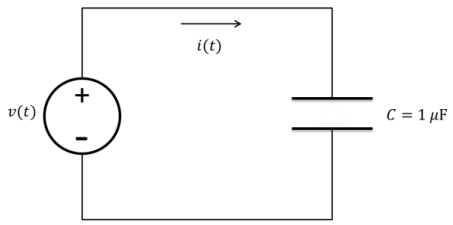
$$q(t) = Cv(t)$$

$$i(t) = \frac{dq(t)}{dt}$$

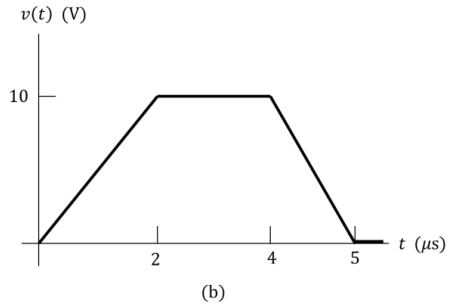
$$i(t) = C\frac{dv(t)}{dt}$$

Ex:

Given *v(t)* as Fig. (b), determine the *i(t)* for the circuit in Fig. (a).

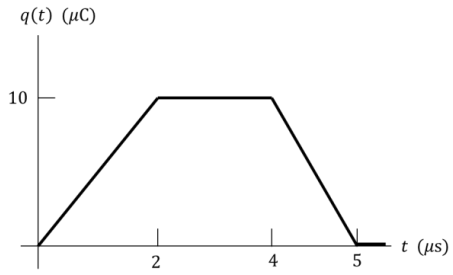


(a)



(b)

$$q(t) = Cv(t) = 10^{-6}v(t)$$



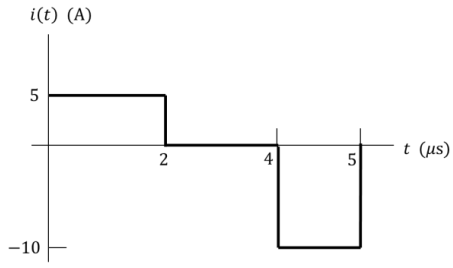
(c)

$$i(t) = C\frac{dv(t)}{dt} = 10^{-6}\frac{dv(t)}{dt}$$

t between 0 and 2 μs

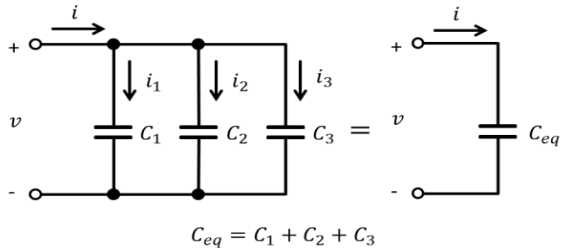
$t = 2$ and 4 μs

between $t = 4$ and 5 μs



(d)

Capacitances in parallel



$$C_{eq} = C_1 + C_2 + C_3$$

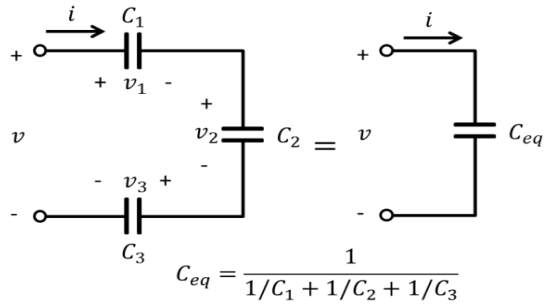
$$i_1 = C_1 \frac{dv}{dt} \qquad i_2 = C_2 \frac{dv}{dt}$$

$$i_3 = C_3 \frac{dv}{dt}$$

By KCL

$$C_{eq} = C_1 + C_2 + C_3$$

Capacitances in series



$$C_{eq} = \frac{1}{1/C_1 + 1/C_2 + 1/C_3}$$

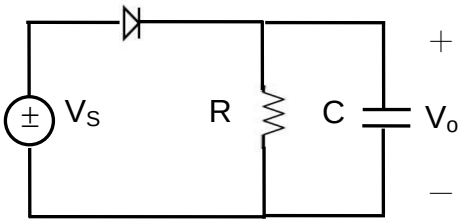
$$v_1 = \frac{q}{C_1} \qquad v_2 = \frac{q}{C_2}$$

$$v_3 = \frac{q}{C_3}$$

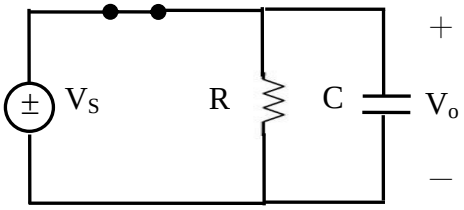
By KVL

$$v = v_1 + v_2 + v_3$$

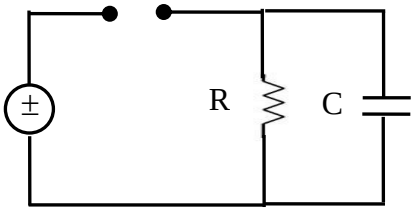
2.1.3: Filter (濾波器)

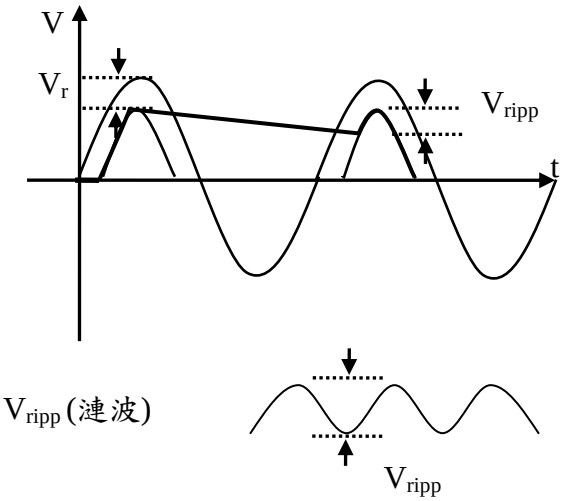


Positive cycle (電容充電)

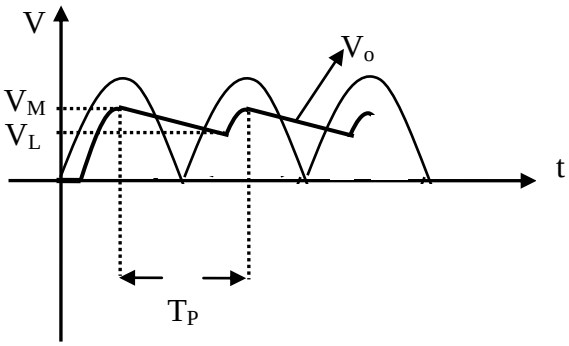


Negative cycle (電容放電)





Quantify the ripple voltage



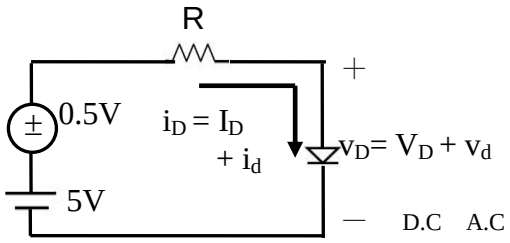
$$PIV: \ half-wave = V_P \quad (no\ filter)$$

$$= 2V_P - V_r - \frac{1}{2}V_{ripp} (with\ filter)$$

$$Full-wave = 2V_P - V_r \quad (no\ filter)$$

$$= 2V_P - V_r \quad (with\ filter)$$

1.4: Diode AC equivalent circuits Ex:



$$i_D = I_S(e^{v_D/nV_T} - 1) = I_S(e^{(V_D+v_d)/nV_T} - 1)$$

$$\cong I_S e^{(V_D+v_d)/nV_T}$$

$$= I_S e^{V_D/nV_T} \bullet e^{v_d/nV_T}$$

$$= I_D \bullet e^{v_d/nV_T} \fallingdotseq I_D(1 + \frac{v_d}{nV_T})$$

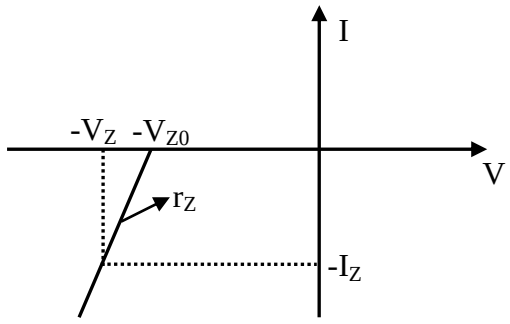
$$= I_D + I_D \bullet \frac{v_d}{nV_T} = I_D + i_d$$

$$r_d = \frac{nV_T}{I_D} \equiv \frac{v_d}{i_d}$$

交流時 Diode models(模型化)成一個電阻 r_d

Voltage regulator (穩壓)

1.5.5: Zener diode (breakdown diode)
(齊納 or 崩潰二極體)



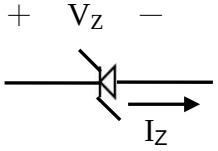
$V_Z = V_{Z0} + I_Z \bullet r_z$

I_{ZK} : knee current

Maxpower : P = IV (I_{Zmax})

I_{ZK} < I_Z < I_{Zmax}

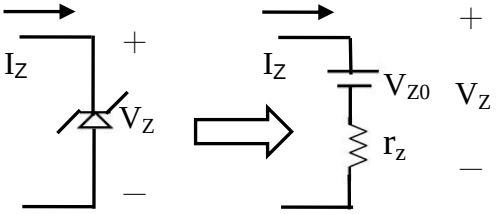
Symbol



D.C model

Open

$V_Z < V_{Z0}$

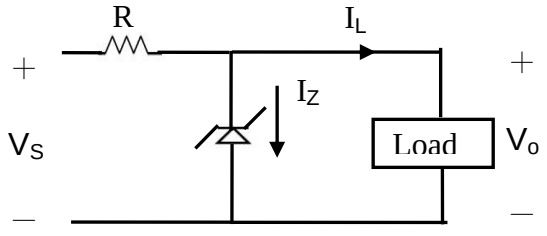


$V_Z \geq V_{Z0}$

$V_Z = V_{Z0} + I_Z \bullet r_Z$

$V_D = V_r + I_D \bullet r_f$

2.2: Zener regulator



$$V_o = \frac{R}{R+r_Z}\bullet V_{Z0} + \frac{r_z}{R+r_z}\bullet V_S - \frac{R\bullet r_Z}{R+r_Z}\bullet I_L$$

V_o 受哪些因素影響 ？

1. 輸入改變(V_S b)
2. 負載改變(I_L b) $\Rightarrow$ $V_o(V_S\ ,\ I_L)$

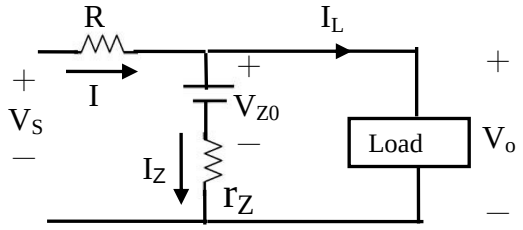
$$\Delta V_o = \frac{R}{R+r_Z}\bullet \Delta V_{Z0} + \frac{r_z}{R+r_z}\bullet \Delta V_S - (R\ /\!/\ r_Z)\Delta I_L$$

$$= \frac{r_z}{R+r_z}\bullet \Delta V_S - (R\ /\!/\ r_Z)\Delta I_L$$

$$\left.\frac{\Delta V_o}{\Delta V_S}\right|_{\Delta I_L=0} = +\frac{r_Z}{R+r_Z}$$

$$line\ regulation \equiv \left.\frac{\Delta V_o}{\Delta V_S}\right|_{\Delta I_L=0}$$

$$load\ regulation \equiv \left.\frac{\Delta V_o}{\Delta I_L}\right|_{\Delta V_S=0}$$

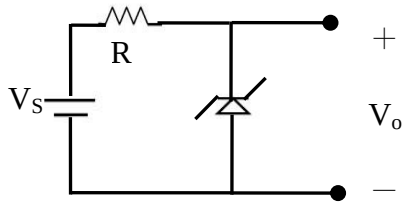


$$\left.\frac{\Delta V_o}{\Delta I_L}\right|_{\Delta V_S=0} = -(R\ /\!/\ r_Z)$$

$$V_o = V_{Z0} + I_Z \bullet r_Z$$
$$= V_{Z0} + (I - I_L)\bullet r_z \qquad \text{..... (1)}$$

$$I = \frac{V_S - V_o}{R} \qquad \text{..... (2)}$$

Ex:
Given zener diode $V_Z = 6.8V$ at $I_{ZT} = 5mA$
$r_z = 20\ \Omega$, $I_{zk} = 0.2$ mA



(a) $V_S = 10$ V, R = 0.5 kΩ, V_o = ?

(b) $\Delta V_S = \pm 1\ V, \quad V_S = 10 \pm 1\ V,\ \Delta V_o = ?$
line regulation = ?

(d) $V_S = 10V, R_L = 2k\Omega \rightarrow 0.5k\Omega,\ V_o = ?$

(c) $V_S = 10, \quad \Delta V_S = 0,$ R=0.5kΩ, $R_L = \infty \rightarrow 2k\Omega$

ΔV_o =? *load regulation*
$\Delta I_L = ?$

(e) $R_L = \infty \rightarrow 2k \rightarrow R_{L\min}$ ⋮ $\rightarrow 0.5k$

Zener 有作用 ⋮ Zener 無作用

求 $R_{L\min}$ (Vs = 10V, ΔVs = ±1V) ?

$$R_{\min} = \frac{V_{S\max} - V_{O\max}}{I_{Z\max} + I_{L\min}}$$

$$R_{\max} = \frac{V_{S\min} - V_{O\min}}{I_{Z\min} + I_{L\max}}$$

$V_S = 10 \pm 0.1V \qquad V_{Z0} = 6.7V$

$r_Z = 20, \quad I_{ZK} \quad or \quad I_{Z\min} = 0.2mA$

$I_{Z\max} = 10mA, \quad I_L = 0 \sim 5mA$

(f) $[R_{\min} \sim R_{\max}]$

$R_{\min} = 0.32k\Omega$

$R_{\max} = 0.615k\Omega$

Ex :
Given zener diode $V_Z = 7.5V$ at $I_{ZT} = 20mA$
$r_z = 10\Omega$, $I_{Zmin}=5mA$, $V_S = 20 \pm 5V$
$I_L = 0\sim15mA$

(a) $R_{\max} = ?$

(b) $V_o\big|_{at\ R\max} = ?$

(c) $\Delta V_{o\max}(due\ to\ V_S \text{ b},\ I_L \text{ b})\big|_{at\ R_{\max}} = ?$

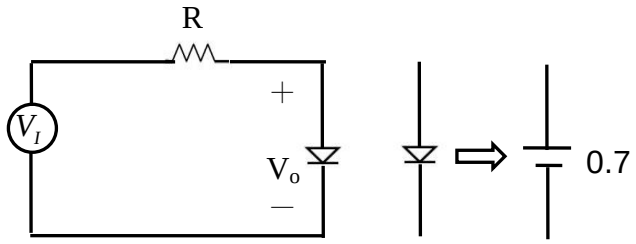
(d) percent regulation = $\dfrac{V_{o\max} - V_{o\min}}{V_{o(\text{nominal})}}$

$= \dfrac{\Delta V_{o\max}}{V_{o(nom)}} \times 100\ \%$

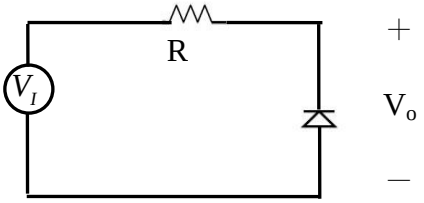
2.3.1: Clipping circuit (截波電流) or
Clipper or limiting circuit

= 將 output 波形限制在某一點以上或以下的電路

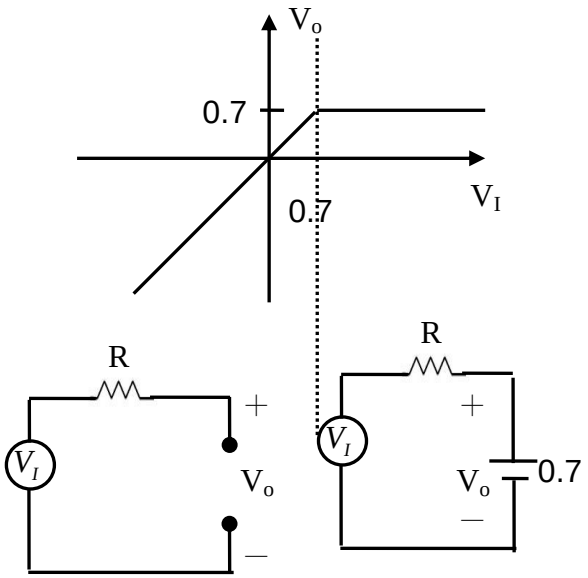
電路



電路



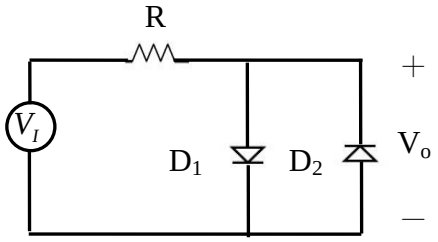
VTC



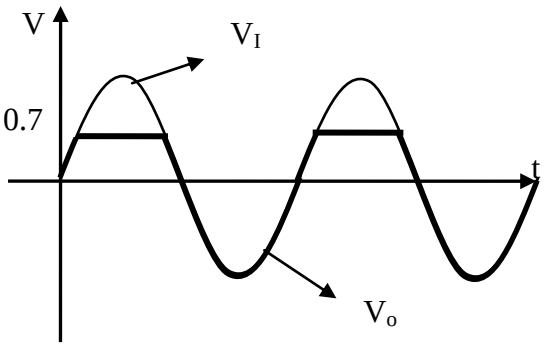
VTC

V_o 波形

電路 (double limiting clipper)

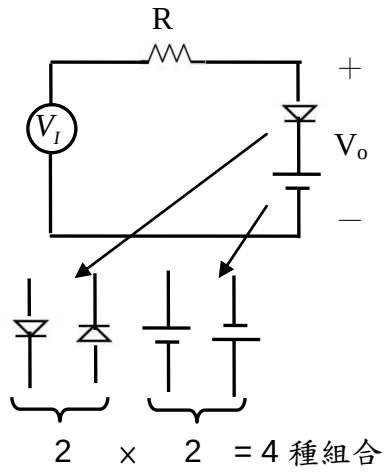


V_o 波形

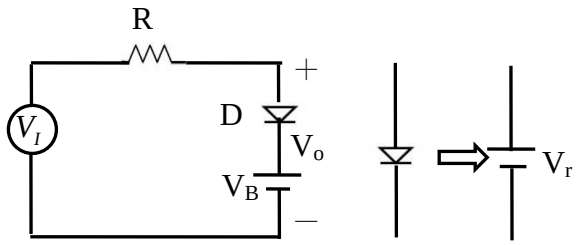


VTC

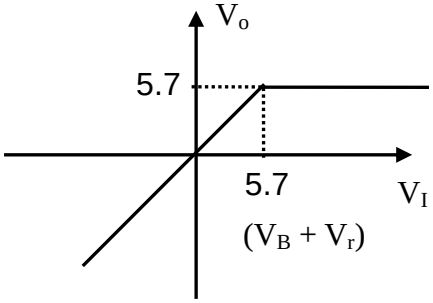
V_o 波形



電路



VTC



(1) $V_I = 0 \quad D_{off} \quad V_o = V_I$

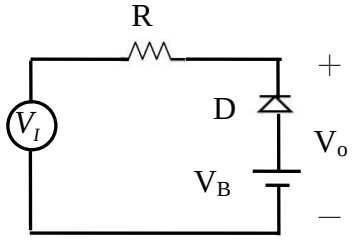
(2) $V_I < 0 \quad D_{off} \quad V_o = V_I$

(3) $V_I = V_B + V_r \quad D_{off \to ON}$

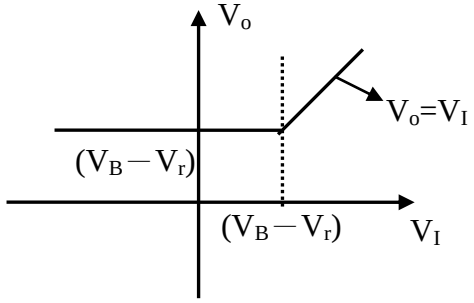
(4) $V_I > V_B + V_r \quad D_{ON} \quad V_o = V_B + V_r$

V_o 波形

電路



VTC



$V_I = 0 \quad D_{ON} \quad V_o = V_B - V_r$

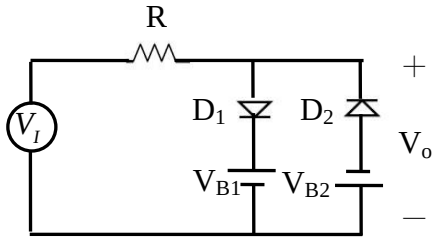
$V_I < 0 \quad D_{ON} \quad V_o = V_B - V_r$

$V_I = V_B - V_r \quad D_{ON \to off}$

$V_I > V_B - V_r \quad D_{off} \quad V_o = V_I$

V_o 波形

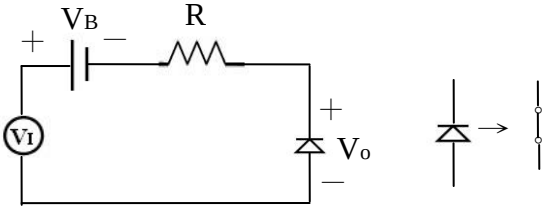
電路



VTC

V_o 波形

電路



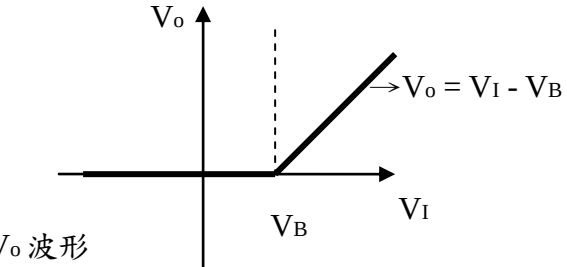
$V_I = 0$ D_{on} $V_o = 0$

$V_I < 0$ D_{on} $V_o = 0$

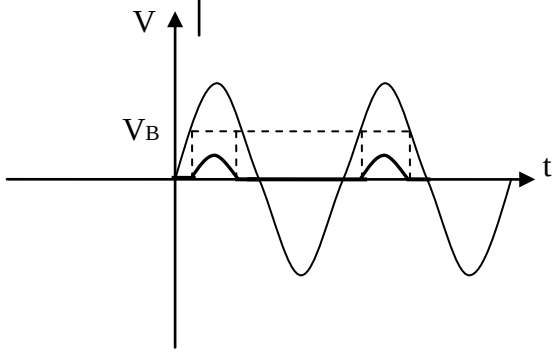
$V_I = V_B$ D_{on} $\rightarrow$ off

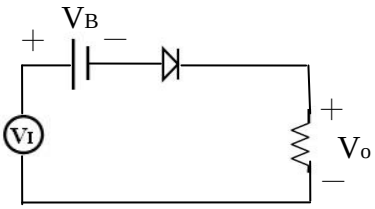
$V_I > V_B$ D_{off} $V_o = -V_B + V_I$

VTC



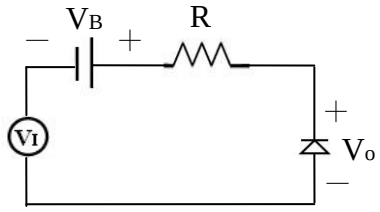
Vo 波形





Same as above

電路



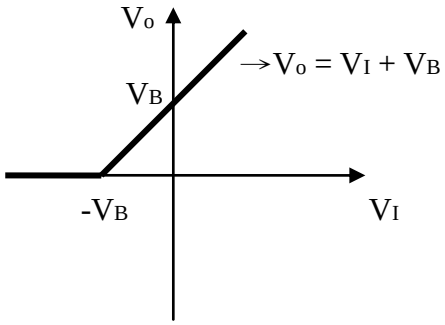
$V_I = 0$ D_{off} $V_o = V_B + V_I = V_B$

$V_I > 0$ D_{off} $V_o = V_B + V_I$

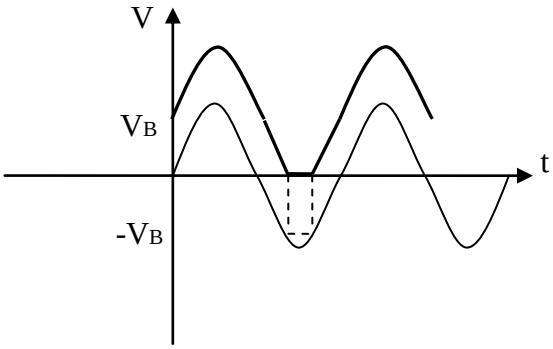
$V_I = -V_B$ D_{off} $\rightarrow$ on

$V_I < -V_B$ D_{on} $V_o = 0$

VTC

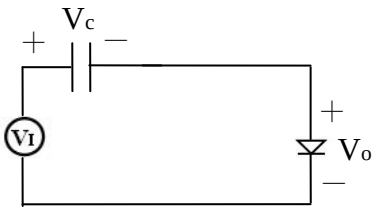


Vo 波形



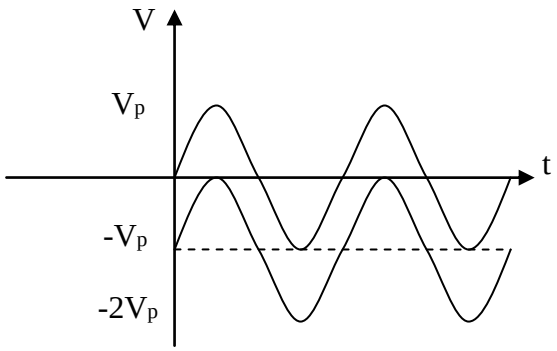
2.3.2: Clamping circuit (箝位電路) or clamper

電路

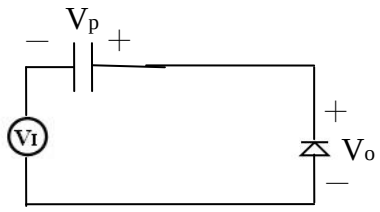


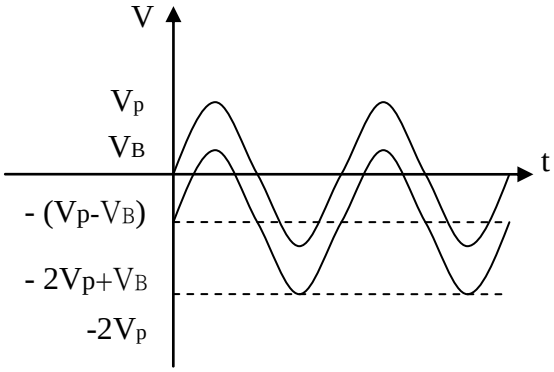
Peak Detector

Vo 波形

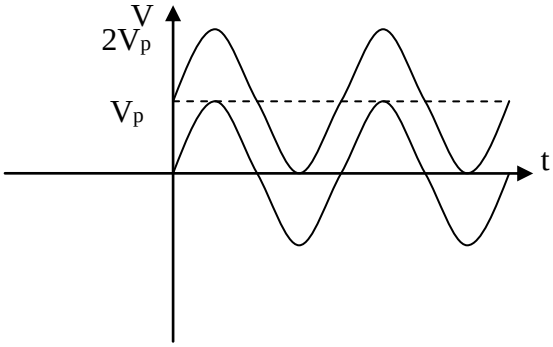


電路

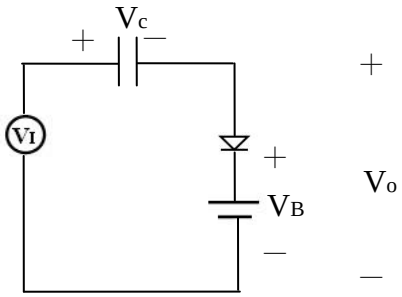




Vo 波形



電路



Don 時　　Vc max = Vp－VB

且維持固定值

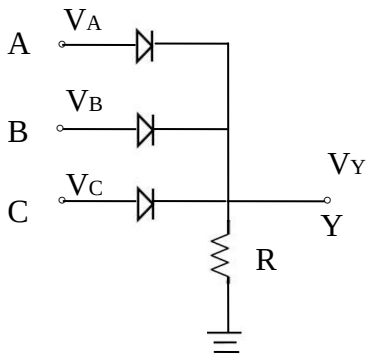
⇨ Vo = -Vc + VI

= - (Vp － VB) + VI

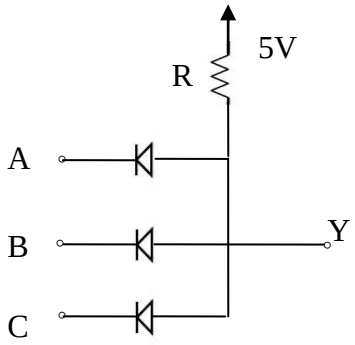
VI = Vp　　Vo = VB

VI = -Vp　Vo = -2Vp + VB

2.4.2: Logic circuit

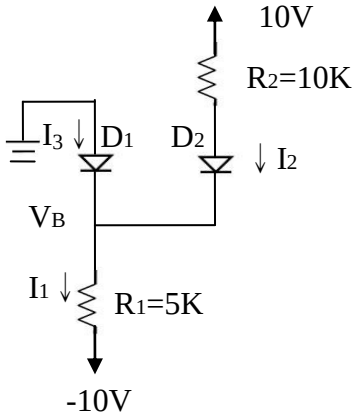


Y = A+B+C (OR gate)



Y = A • B • C (AND gate)

2.4.1: Multiple-diode circuit



Assume D_1, D_2 為 ideal diode, 求 I_1, I_2, V_B = ?

D_1, D_2 不是 ON,就是 OFF, 4 種組合

ON → short

OFF → open

解法步驟

① 先假設 Diode 的 state

ON → short

OFF → open

② 依照假設的情形,來解電路

③ 驗證結果是否與假設相符

if 假設 ON 要有 $I_D > 0$, $V_D > 0$ 的結果;

otherwise 改設為 OFF;

if 假設 OFF 要有 $I_D = 0$, $V_D < 0$ 的結果;

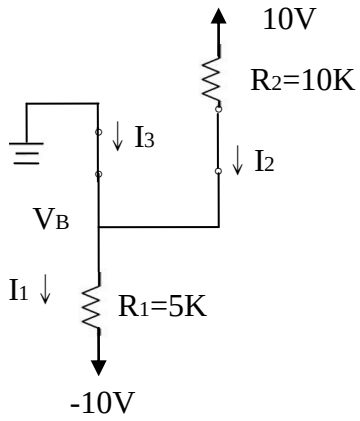
otherwise 改設為 ON;

④ 修正假設,再解一次②

Sol:

Assume D_1, D_2 均為 ON

D_1, D_2 => short



$V_B = 0$

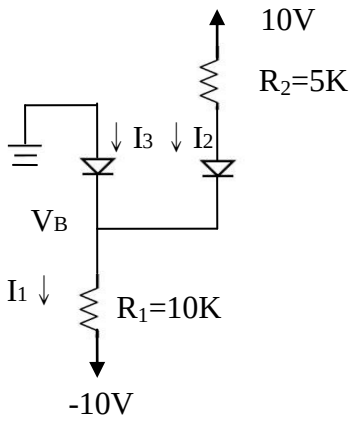
$I_1 = [0-(-10)]/5K = 2mA$

$I_2 = (10-0)/10K = 1mA$

$I_3 = I_1 - I_2 = 1mA$

D_1, D_2 的電流均 > 0, 猜對

Ex

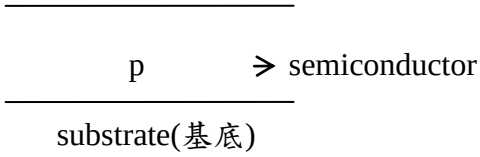


5.1: Field-Effect Transistors (FETs)
場效電晶體

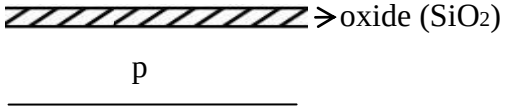
MOSFETs (Metal-Oxide-Semiconductor)

MOS : 由結構而來
FET : 由作用機制而來

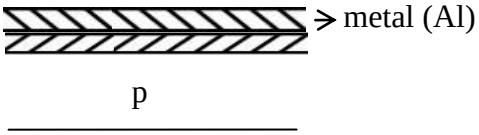
①



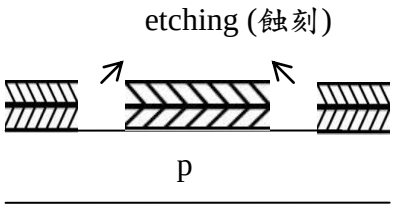
②



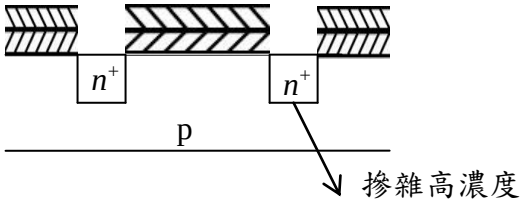
③



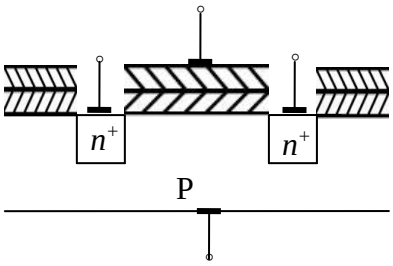
④



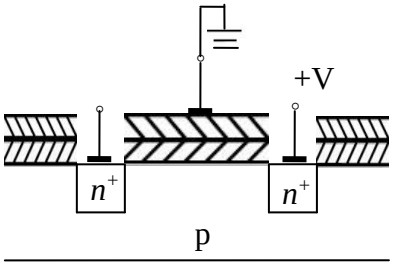
⑤



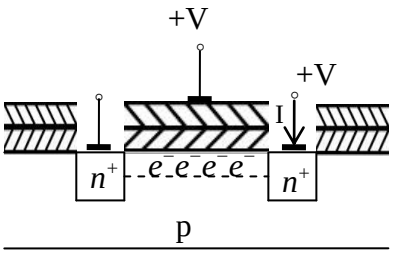
⑥

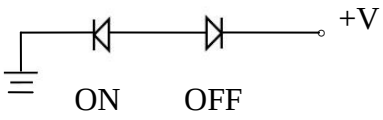


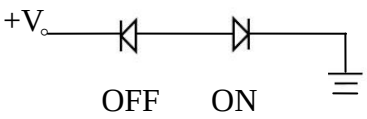
How does MOSFET work?



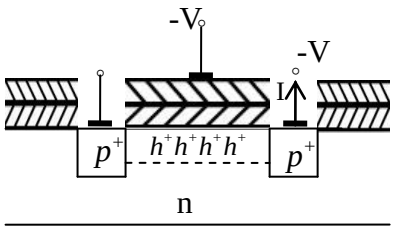
“electron inversion layer” (電子反轉層) or n channel (通道)

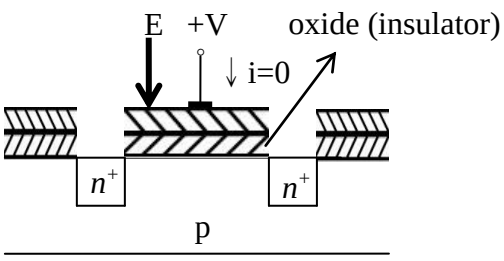






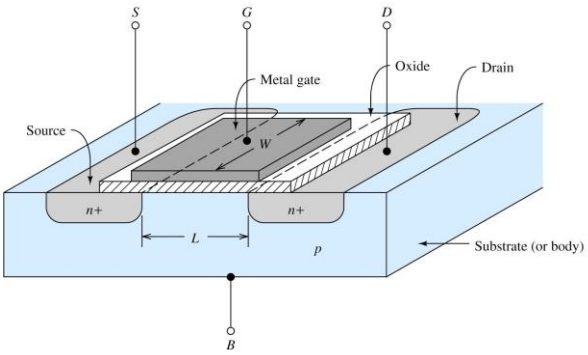
N channel MOS (NMOS)



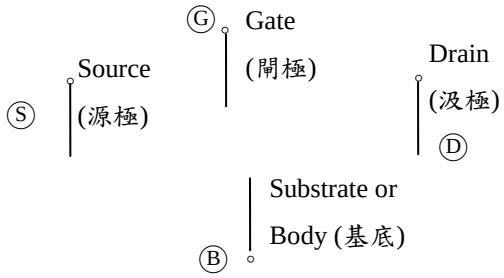


“hole inversion layer” (電洞反轉層) or p channel

P channel MOS (PMOS)



Terminal 命名



nmos { enhancement mode / depletion mode

pmos { enhancement mode / depletion mode

enhancement mode:
外加 gate 電壓,使 channel 形成

depletion mode:
通道已形成,外加 gate 電壓,改變 channel 厚度

V_{DS} 的極性
NMOS, $V_{DS} > 0$ (將電子拉出來)
PMOS, $V_{DS} < 0$ (將電洞拉出來)

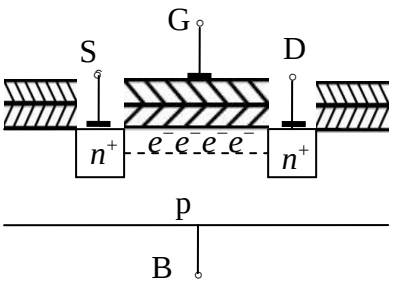
S 提供 carrier

nmos s 提供 e^-
pmos s 提供 h^+

B 的極性
NMOS B 接(-)
PMOS B 接(+)
$V_{GS} > 0$ for nmos 讓反轉層形成

Enhancement n-type MOSFET

(Enhancement NMOS)



Gate 電壓：①正負要對②大小要夠

才能產生 channel

$V_{TN} \equiv V_{GS}$ 使得 channel 剛好產生

↙

nmos (Threshold Voltage 臨界電壓)

$\frac{\in_{ox}}{t_{ox}} \equiv$ C_{ox} (單位面積的氧化層電容)

[Cox] = F/cm^2

MOS Symbol

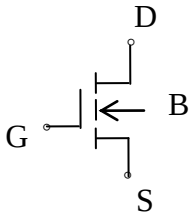
V_{TN} = ? 1, 2, or 3V

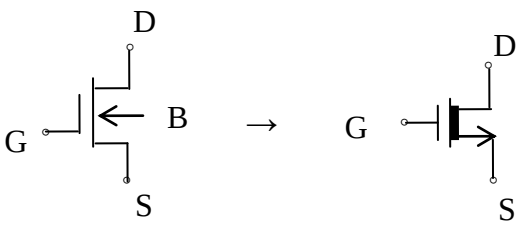
影響 V_{TN} 大小的因素

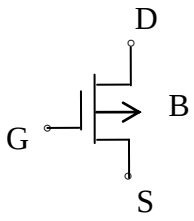
① t_{ox} (Oxide thickness)

② ε_{ox} (Oxide permittivity)

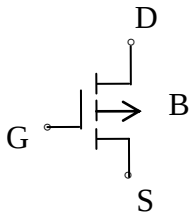
③ N_A in substrate







① $V_{GS} < V_{TN}$ $i_D = 0$, $i_S = 0$
cutoff (截止區)



② $V_{GS} \geqq V_{TN}$ 有通道產生
再外加 V_{DS} 會有電流

ⓐ V_{DS} 很小

I-V 特性曲線

I： i_D = ? i_S = ? i_G = ?

V：V_{GS} = ? V_{DS} = ?

$i_G = 0$

$i_D = i_S$

$i_D = f(V_{GS}, V_{DS})$

$= f((V_{GS} - V_{TN}), V_{DS})$

$V_{eff} \equiv V_{GS} - V_{TN}$

i_D = ?

ⓑ V_{DS} ↑↑　$V_{DS} \leqq V_{GS} - V_{TN}$

pinched-off (夾止)

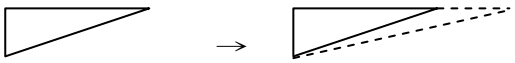
$$i_D = \mu_n C_{ox} \frac{w}{L}(V_{GS} - V_{TN})V_{DS}$$

$$r_{DS} = \frac{V_{DS}}{i_D} = 1 \ / \ \mu_n C_{ox} \frac{w}{L}(V_{GS} - V_{TN})$$

$$\mu_n C_{ox} \equiv \kappa_n'$$

$$i_D = \kappa_n' \frac{w}{L}[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2]$$

ⓒ $V_{DS} \geqq V_{GS} - V_{TN}$



$$i_D = \kappa_n' \frac{w}{L}[(V_{GS} - V_{TN})V_{DS} - \frac{1}{2}V_{DS}^2]$$

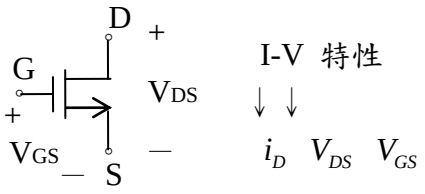
$$= \frac{1}{2}\mu_n C_{ox} \frac{w}{L}[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$$= \kappa_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

$$\kappa_n = \frac{1}{2}\mu_n C_{ox} \frac{w}{L} \text{ (conduction parameter)}$$

MOS 工作在 triode region (三極體區) or non-saturation region

Summary



$i_D = \kappa_n (V_{GS} - V_{TN})^2$

MOS 工作在 saturation region (飽和區)

① $V_{GS} < V_{TN}$ Q : cutoff

$i_D = i_S = i_G = 0$

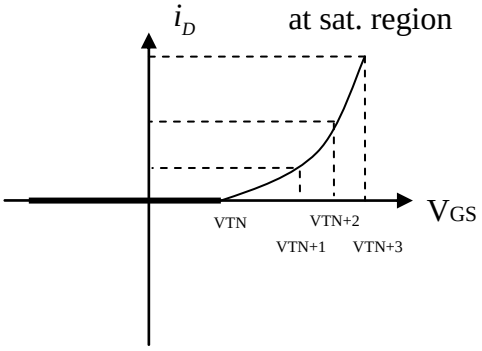
② $V_{GS} \geqq V_{TN}$ Q : conducting { ⓐ triode ; ⓑ sat.

ⓐ $V_{DS} \leqq V_{GS} - V_{TN}$

$$i_D = \kappa_n [2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

ⓑ $V_{DS} \geqq V_{GS} - V_{TN}$

$$i_D = \kappa_n (V_{GS} - V_{TN})^2$$



Ex:

enhancement nmos $V_{TN} = 1.2V$, $V_{GS} = 2V$

$\mu_n = 500\, cm^2 / V \bullet S$, $\varepsilon_{ox} =$

$(3.9)(8.85\times10^{-14})$F/cm

$t_{ox} = 450$Å, W = 100 μm, L = 7 μm 求 i_D

when (a) $V_{DS} = 0.4V$ (b) $V_{DS} = 1V$ (c)$V_{DS} = 5V$

Sol:

$$\kappa_n = \frac{1}{2}\mu_n C_{ox}\frac{w}{L} =$$

$$\frac{1}{2}\cdot 500 \cdot \frac{(3.9)(8.85\times10^{-14})}{450\times10^{-10}\times10^{2}}\cdot\frac{100}{7} =$$

$0.274 mA/V^2$

(a) $V_{DS} = 0.4 < (2-1.2) = 0.8V$, at triode region

$i_D =$

$= 0.132mA$

(b) $V_{DS} = 1 > 0.8$, at sat region

$i_D =$

$= 0.175mA$

(c) $V_{DS} = 5 > 0.8$, at sat region

$i_D = 0.175mA$

Ex:

Output resistance $r_0 \equiv (\frac{\partial i_D}{\partial V_{DS}})^{-1}|_{\text{VGS = const}}$

非理想 I-V 特性曲線
Early Effect (厄立效應) or
Channel length modulation
(通道長度調變)

$r_0 = [\lambda \kappa_n (V_{GS} - V_{TN})^2]^{-1}$

Ex:
nmos enhancement device, $V_{TN} = 0.8V$

$\kappa_n = 0.1mA/V^2$, $V_{GS} = 2.5V$, $\lambda = 0.02V^{-1}$

$V_{DS} = 2V$, 求 i_D 及 r_0

$i_D = \kappa_n (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$

$\lambda = \frac{1}{V_A}$, $V_A \equiv$ Early voltage

Subthreshold conduction (次臨界導通)

3. Oxide breakdown

Breakdown

1. pn junction breakdown

Body Effect (基體效應)

$V_{SB} \neq 0$ 影響 V_{TN} 之大小

2. punch-through

Ex:

V_{TN0}=1V, γ=0.35$V^{\frac{1}{2}}$, ϕ_f=0.35V

求 V_{TN} at (a)V_{SB} = 0V (b)V_{SB} = 1V

$$V_{TN} = V_{TN0} + \gamma\left[\sqrt{2\varphi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

Reason:

溫度效應

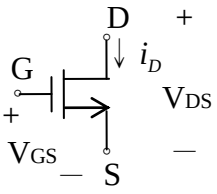
T↑, i_D↓

Negative feedback (負回授)

I-V characteristics for other types of MOS

- nmos
  - enhancement
  - depletion
- pmos
  - enhancement
  - depletion

"enmos"



n channel V_{TN} (吸電子形成 channel)

=>V_{TN}(+)

V_{DS}(把通道的電子吸出去，i_D 相反方向)

=>V_{DS}(+)

$\lambda = \frac{1}{V_A}$ (+)

V_{GS}<V_{TN}, cutoff, (原來的 channel 消失了) i_D =0

V_{GS}>V_{TN}, conducting, (V_{GS} 可(＋)可(－))

① $V_{DS} \leqq V_{GS} - V_{TN}$ (triode region)

$$i_D = \kappa_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

② $V_{DS} \geqq V_{GS}$-V_{TN} (sat. region)

$$i_D = \kappa_n(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

$V_{GS} < V_{TN}$, cutoff, $i_D = 0$

$V_{GS} > V_{TN}$, conducting

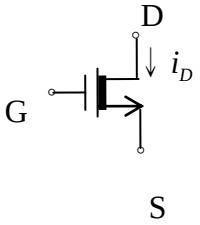
①$V_{DS} \leqq V_{GS}$-V_{TN} (triode region)

$$i_D = \kappa_n[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2]$$

②$V_{DS} \geqq V_{GS}$-V_{TN} (sat. region)

$$i_D = \kappa_n(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

"dnmos"



V_{GS} = 0 時，已有 channel 存在，V_{TN} 為使 channel 剛要形成的電壓(V_{GS})

=>V_{GS} 要加(-)的,將 n channel 的 e^- 趕走

=>V_{TN}(－)

=>V_{DS}(＋)(吸引電子)

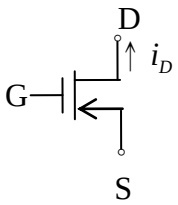
=> $\lambda = \frac{1}{V_A}$ (+)

V_{GS} = 0, i_D 稱 I_{DSS}

Ex:

Ex:

"epmos"



p channel V_{TP}(吸電洞形成 channel)

=>V_{TP}(－)

V_{DS}(把 channel 中的電洞吸出去，i_D 相同方向)

=>V_{DS}(－)

$\Rightarrow \lambda = \frac{1}{V_A}$(－)

$V_{GS} > V_{TP}$, cutoff, $i_D = 0$

(不夠負)

$V_{GS} < V_{TP}$, conducting

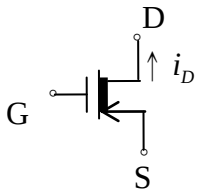
① $V_{DS} \geqq V_{GS}$-V_{TP} (triode region)

$$i_D = \kappa_p[2(V_{GS} - V_{TP})V_{DS} - V_{DS}^2]$$

② $V_{DS} \leqq V_{GS} - V_{TP}$ (sat. region)

$$i_D = \kappa_p(V_{GS} - V_{TP})^2(1 + \lambda V_{DS})$$

"dpmos"



P channel 有電洞 V_{GS} 加(＋)將電洞趕走

=>V_{TP}(＋)

=>V_{DS}(－) (把電洞吸出去)

$\Rightarrow \lambda = \frac{1}{V_A}$(－)

$V_{GS} > V_{TP}$, 原有的 channel 消失了, $i_D = 0$, cutoff

$V_{GS} < V_{TP}$, conducting

① $V_{DS} \geqq V_{GS}$-V_{TP} (triode region)

$$i_D = \kappa_p[2(V_{GS} - V_{TP})V_{DS} - V_{DS}^2]$$

② $V_{DS} \leqq V_{GS} - V_{TP}$ (sat. region)

$$i_D = \kappa_p(V_{GS} - V_{TP})^2(1 + \lambda V_{DS})$$

Summary

四種 mos, i_D 公式均相同, 差別是判斷方式, nmos 和 pmos 相反

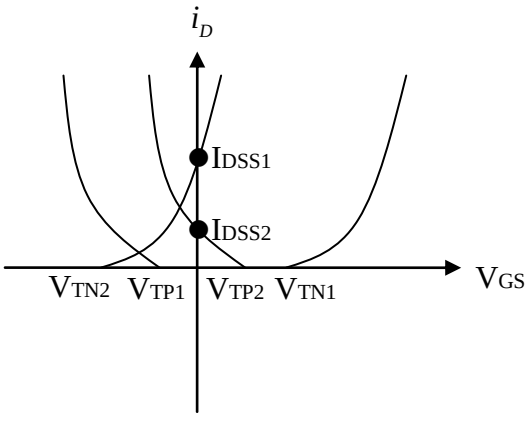
① cutoff 與 conducting 相反

$V_{GS} \begin{matrix} \geq \\ \leq \end{matrix} V_T$ 之關係

② triode 與 sat region 相反

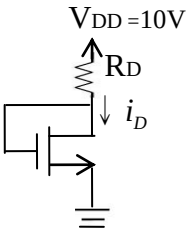
$V_{DS} \begin{matrix} \geq \\ \leq \end{matrix} (V_{GS}-V_T)$之關係

Ex:



MOS DC Analysis

Ex1:



enmos

i_D = 0.4mA 求 R_D=?

Given V_{TN}=2V

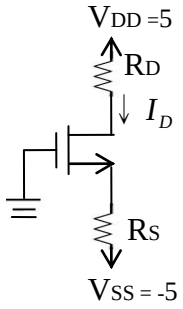
$\kappa_n' = 20\mu A/V^2$

W = 100 μm, L = 10 μm

λ = 0

Sol:

Ex2:



enmos

I_D=0.4mA, VD=1

求 RD=? RS=?

Given VTN = 2V,

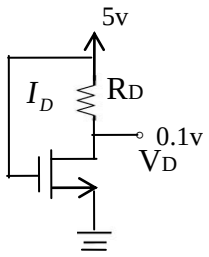
$\kappa_n' = 20 \mu A/V^2$

L = 10 μm, W = 400 μm

λ = 0

Sol:

Ex3:



enmos

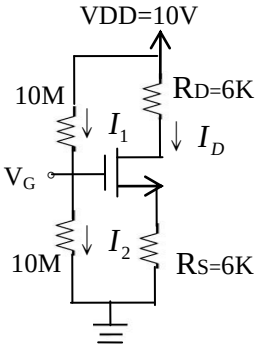
VD=0.1V, 求 RD

Given VTN = 1

$\kappa_n = 0.5 mA/V^2$

Sol:

Ex4:



分析此電路

(求出所有電壓, 電流)

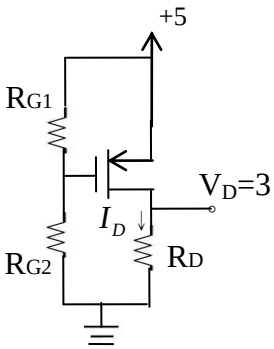
Given VTN = 1V

$\kappa_n = 0.5 mA/V^2$

λ = 0

Sol:

Ex5:



epmos

Given $V_{TP} = -1V$

$\kappa_p = 0.5 \, mA/V^2$

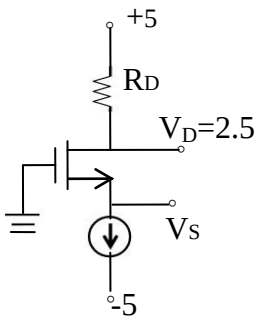
$\lambda = 0$

(a) design R_{G1}, R_{G2}, R_D such that Q at sat. region, and $I_D = 0.5mA$, $V_D = 3V$

(b) 使 Q 在 sat. region 的 R_{Dmax} = ?

Sol:

Ex6:



enmos

Given V_{TN} = 0.8V

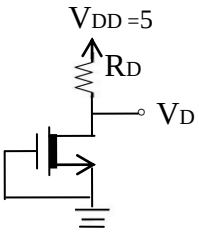
$\kappa_n' = 80\,\mu A/V^2$

W/L = 3, design R_D such that I_D=250 μA

V_D = 2.5V. What's Vs = ?

Sol:

Ex7:



dnmos

given $\kappa_n' = 20\,\mu A/V^2$

V_{TN} = -1V

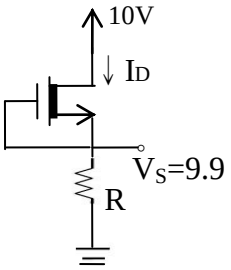
λ = 0

(a) 求 W/L=? such that I_D=100 μA at sat.

(b) R_D range? in (a)

Sol:

Ex8:



dnmos

given $\kappa_n = 0.5\, mA/V^2$

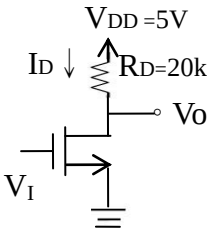
V_{TN} = -1V

求 R such that

V_S = 9.9V

Sol:

Ex9:



enmos

$\kappa_n = 0.1\, mA/V^2$

V_{TN}=0.8V

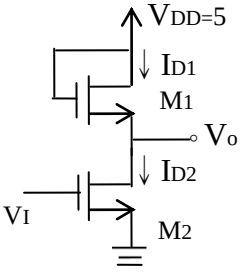
求 Vo , I_D if

(a) V_I = 0

(b) V_I = 5V

Sol:

Ex10:



$V_{TN1} = V_{TN2} = 1V$

$\kappa_{n1} = 10\,\mu A/V^2$

$\kappa_{n2} = 50\,\mu A/V^2$

求 V_o, I_{D1} if

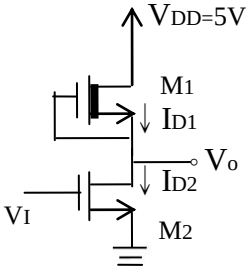
(a) $V_I = 5V$

(b) $V_I = 1.5V$

(c) $V_I = 0$

Sol:

Ex11:



$V_{TN1} = -2V$

$V_{TN2} = 1V$

$\kappa_{n1} = 10\,\mu A/V^2$

$\kappa_{n2} = 50\,\mu A/V^2$

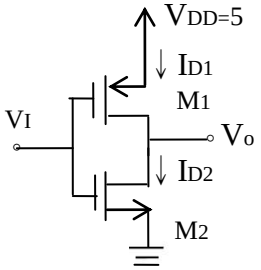
求 Vo & I_D if

(a) $V_I = 5V$

(b) $V_I = 0$

Sol:

Ex12:



$\kappa_n = \kappa_p = 1 mA/V^2$

V_{TN} = 1V V_{TP} = -1V

求 V_o 及 I_{D1} if

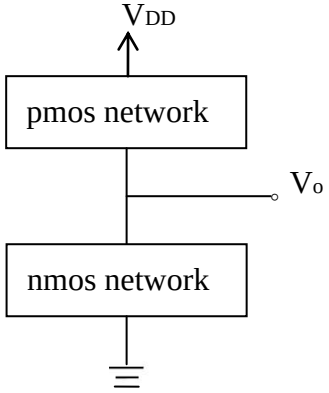
(a) V_I = 0

(b) V_I = 5V

Sol:

Complementary MOS (CMOS)

CMOS logic gate design

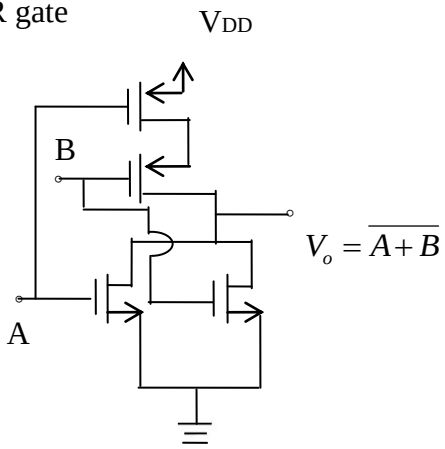


CMOS inverter

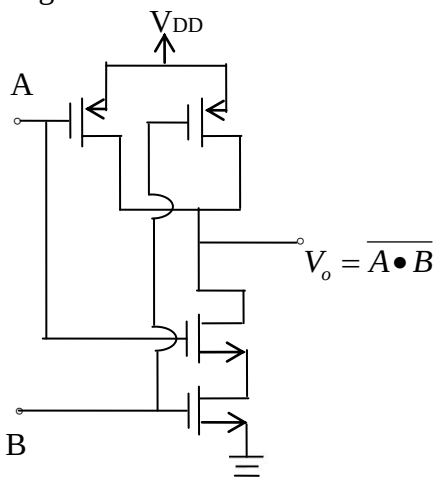
V_I = high, nmos ON, pmos OFF, V_o = low

V_I = low, nmos OFF, pmos ON, V_o = high

NOR gate



NAND gate



Example:

$$F = \overline{A \cdot B + C \cdot D}.$$

Sol:

1. (**n**-network): **Invert** *F* to derive *n*-network

$$(\overline{F} = A \cdot B + C \cdot D)$$

2. (**n**-network): Make connections of transistors:

AND ⇔ Series connection

OR ⇔ Parallel connection

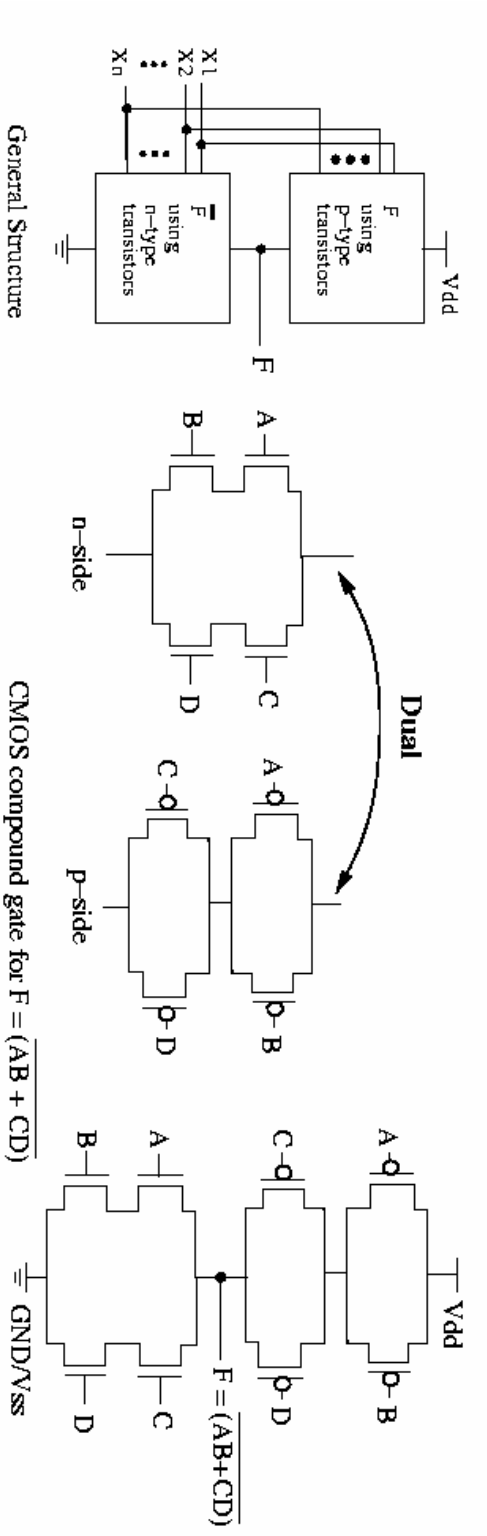
3. (**p**-network): Expand *F* to derive *p*-network

$$(F = \overline{AB + CD} = \overline{AB} \cdot \overline{CD} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D}))$$

each input is inverted

4. (**p**-network): Make connections of transistors (same as step 2)

5. Connect the *n*-network to GND (typically, 0V) and the *p*-network to VDD (5V, 3.3V, or 2.5V, etc)



Ex:

Implement $F = A \cdot B + C \cdot (D + E)$ by CMOS logic.

Sol: