CHAPTER 5

IMPLEMENTATION AND EXPERIMENTAL RESULTS

5.1 Introduction

From the previous chapters, it is seen that the proposed adjustable speed controller basically consists of a conventional popular PI controller coordinated with a PLL controller through weighting factor *k* to achieve both fast transient response and stable speed tracking capability as well as excellent speed accuracy. Theoretically, it seems that through application of the complete three-phase PMBLDC motor phase current information and the high performance PLL control, the proposed adjustable speed drive may incur much higher cost. However, as can be observed later in this chapter, by using the low cost current sensing technique taking advantage of the available low cost Hall-sensor signals and the proposed sophisticated system integration scheme, the resulting cost of the controller is in fact rather competitive with the existing ones. In addition, the proposed controller is almost applicable for ASIC implementation for mass production to decrease the cost greatly. As an illustration of the feasibility and effectiveness of the proposed PLL assisted speed controller for PMBLDC motors, an industrial blower is chosen as the test load. Also, a prototype system is constructed by using a self-designed PMBLDC motor. Detail

implementation of the drive system and experimental results will be shown in the following sections.

5.2 Description of the Test Drive System

The basic configuration of the test system is shown in Fig. 5.1. From Fig. 5.1 one can see that the test system in addition to a personal computer, a digital oscilloscope and a wattmeter for measurement and parameter identification, there are mainly four components. First, an industrial blower with 24” diameter blades and 1100rpm speed rating is chosen as the test load. The second component is a self-designed PMBLDC motor with 6-poles, Y connected winding, 18-slots and with a current rating of 3.5A as well as a trapezoidal phase voltage peak of 150V at 1100rpm rating. It is mainly designed to replace the three

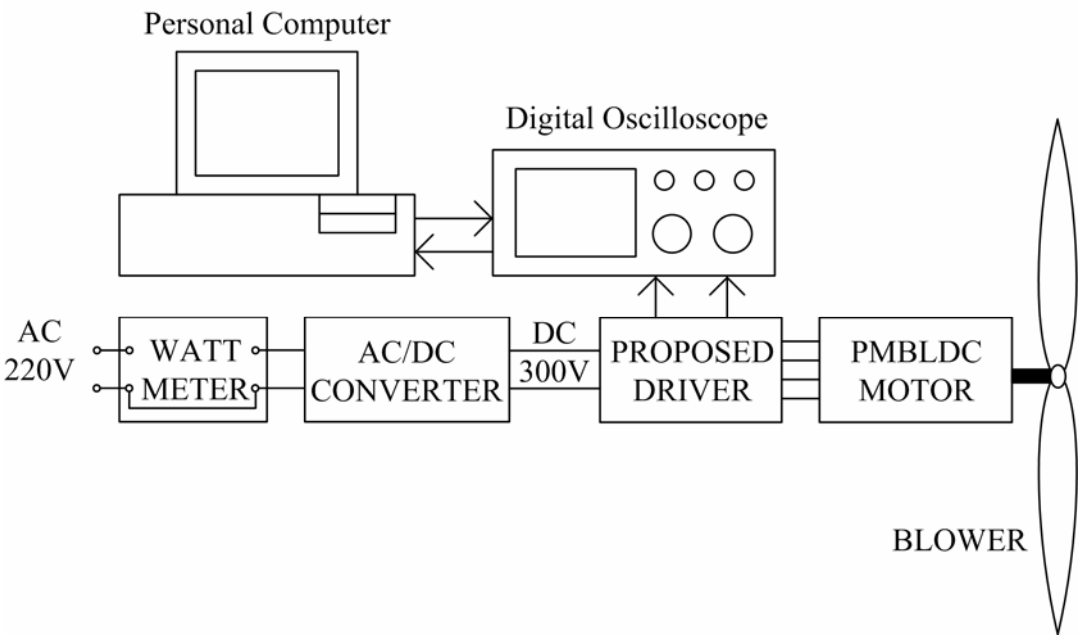
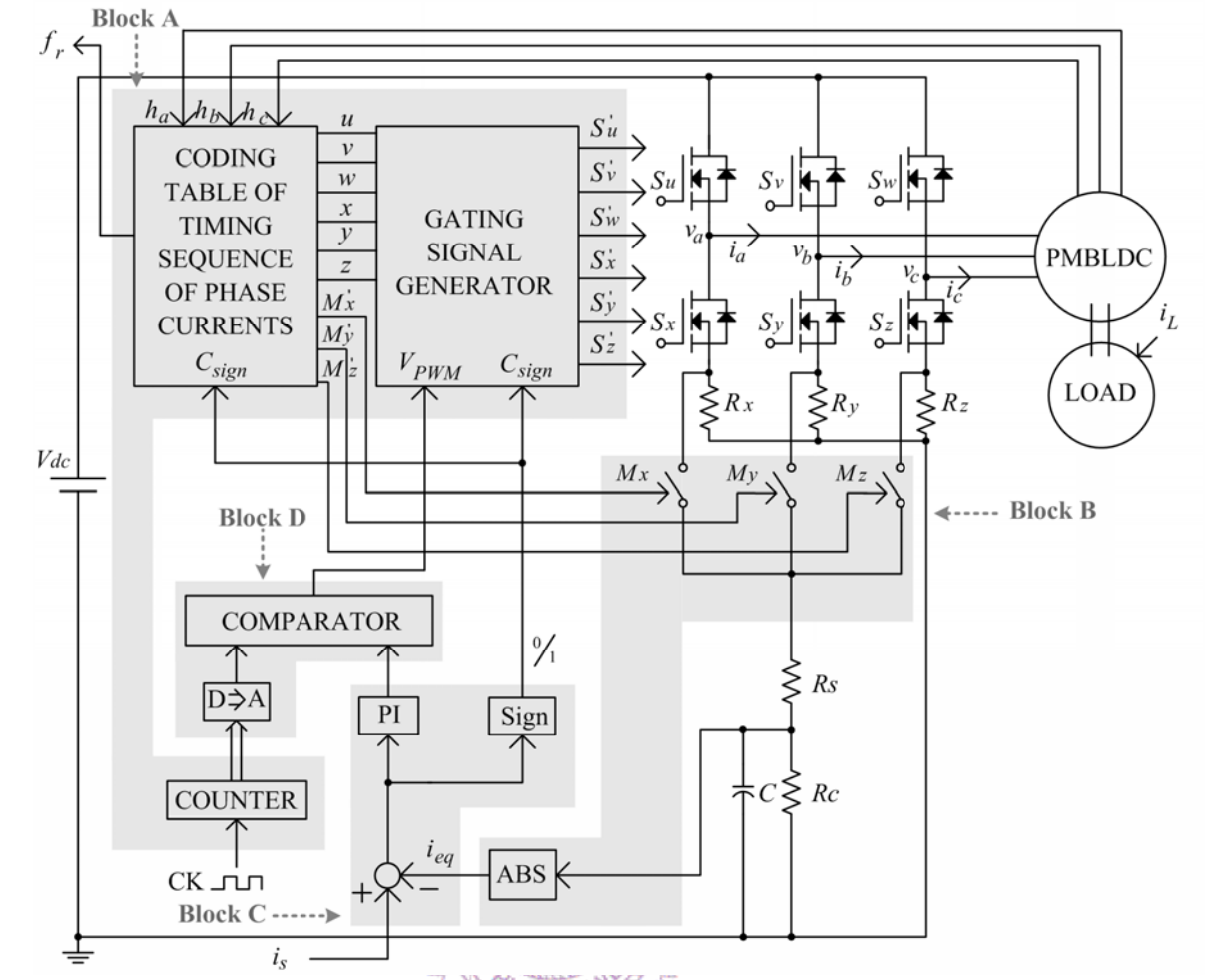


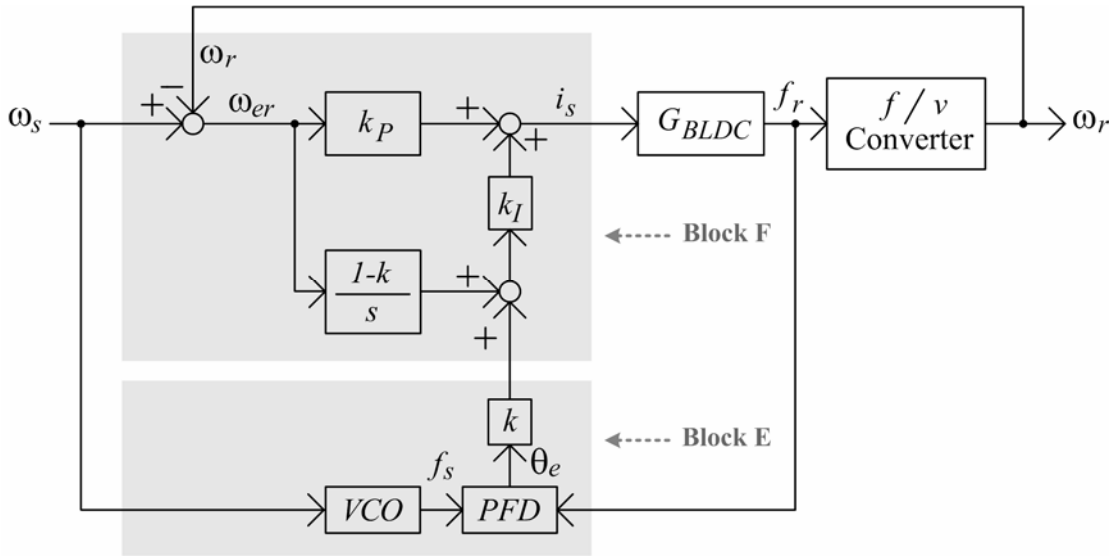
Fig. 5.1 Configuration of the test system.

phase induction motor of the original drive of the industrial blower. Some more detailed information about this PMBLDC motor is given in the Appendix B for reference. The third component is the proposed drive which consists of both power circuits and control circuits. For convenient reference, Fig. 5.2 shows the major contents of the proposed drive as can be seen from Figs. 3.8 and 4.1 respectively.

The power circuits basically consist of a three-phase full bridge inverter with 300V dc input, as can be seen in Fig. 5.2(a) and a Flyback dc power supply with ±15V and +5V outputs for the related control circuits of the proposed drive. As to the control circuits, they are composed of a digital signal circuit and some analog signal circuits. The digital signal circuit part of the proposed drive is marked as Block A as shown in Fig. 5.2(a). It is implemented using a single CPLD chip, namely EPM7064. By using the inputs of Hall-sensor signals (h_a, h_b, h_c), C_{sign} and V_{PWM}, six gating signals (*Su', Sv', Sw', Sx', Sy', Sz'*) are generated for controlling the six active switches of the inverter and additional three control signals are generated for controlling the three transmission gates (*Mx', My', Mz'*). Also, the rotor speed pulse train signal (f_r) is generated for the PLL controller. The analog circuits of the proposed drive include two major parts, namely the current controller analog circuits as shown in Fig. 5.2(a), and the speed controller analog circuits as shown in Fig. 5.2(b). From Fig. 5.2(a) one can see that the current controller analog circuits consist of three blocks, namely Block B for synthesizing the i_{eq} signal, Block C for generating



(a)

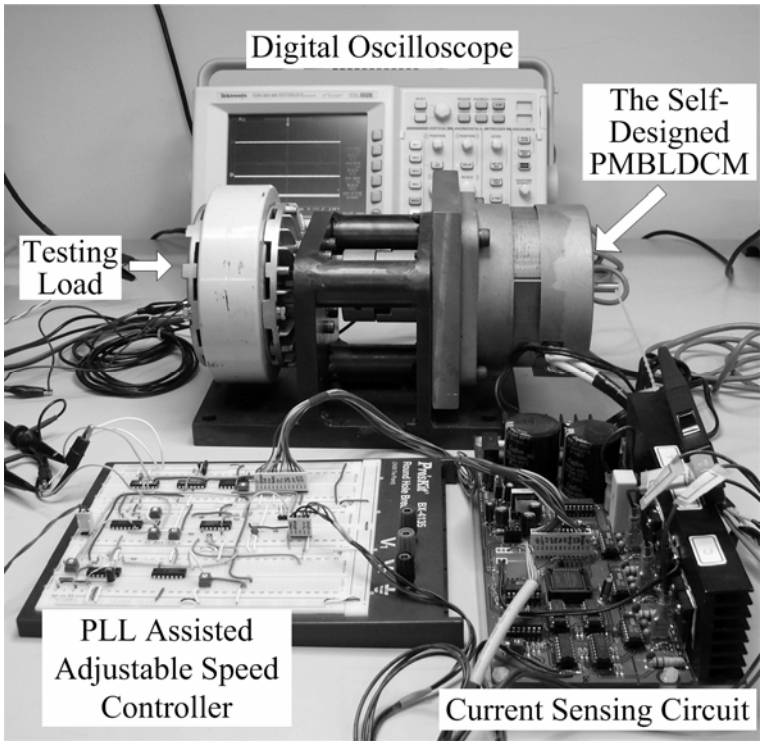


(b)

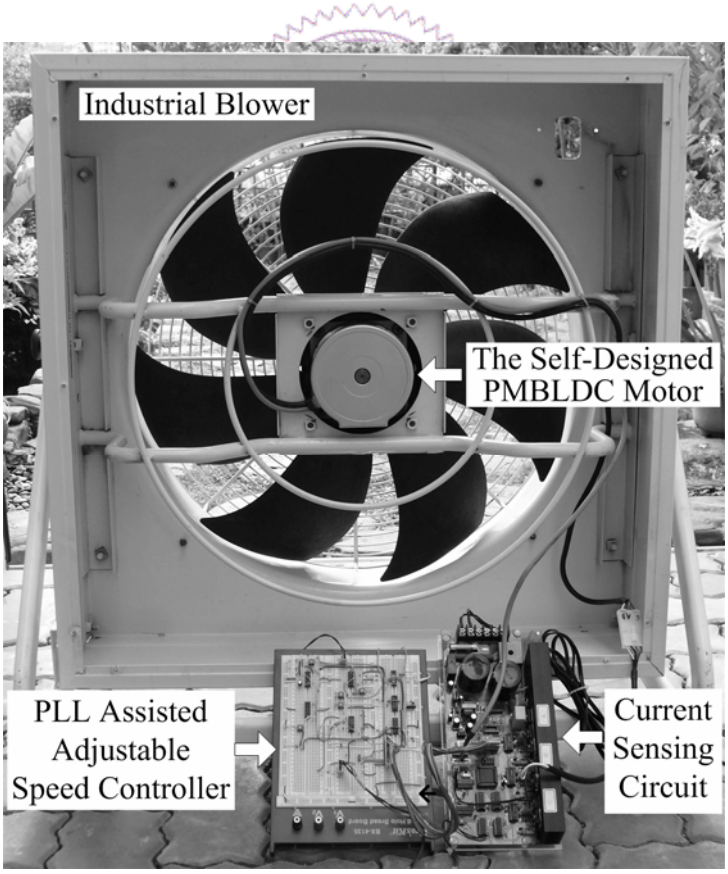
Fig. 5.2 The schematic diagram of the proposed drive. (a) current controller. (b) speed controller.

the (i_s - i_{eq}) signal, which in fact include the sign of (i_s - i_{eq}), namely C_{sign}, as well as its corresponding control signal magnitude, and Block D for generating V_{PWM} signal. From Fig. 5.2(b), one can see that the speed controller analog circuits consist of two blocks, namely Block E for implementing the PLL controller and Block F for implementing the PI controller.

The fourth component of Fig. 5.1 is a low cost diode bridge AC/DC converter which converts a single phase 220V ac into a 300V dc voltage for the following inverter. From Fig. 5.1 one can see that a wattmeter, namely PROVA WM-01 power analyzer is adopted to measure the power consumption, and a digital oscilloscope namely Tektronix TDS3014B, for signal waveform display. As to the PC in Fig. 5.1, it is used for the plant parameter identification. In fact, a software, namely WaveStar installed in PC is used as an interface between the PC and the scope. Thus, both the unit step command and the corresponding step response of the test system can be displayed in the digital scope and sent to the PC for parameter identification using MATLAB software. For providing a better view, Fig. 5.3 shows the completed prototype system where for preliminary testing a magnetic powder clutch is first chosen as the test load in Fig. 5.3(a) and finally an industrial blower as shown in Fig. 5.3(b) is used as the test load for evaluating the energy saving effect.



(a)



(b)

Fig. 5.3 The completed prototype system (a) With a magnetic powder clutch test load. (b) With an industrial blower test load.

5.3 Implementation of the Proposed Drive System

With understanding of the whole system picture as described in the previous section, more details of the implementation of the proposed drive systems can be descried as follows.

First consider the implementation of the corresponding power circuits. Fig. 5.4 shows the hardware realization of the AC/DC converter and the three-phase full bridge inverter at the upper half. From Fig. 5.4 one can see that a low cost diode bridge (BR86D) and two filtering capacitors (C5 and C6) with 1500 μF /200V rating are adopted to provide a dc output of 300V. In order to prevent the inrush current during start up period, a 200 Ω resistor (R52) is inserted in series with the full diode bridge. Also to provide a universal AC/DC converter switch J6 is adopted as an ac power input adjuster for selecting either 110V or 220V ac power. Following the 300V dc voltage is the three-phase full bridge inverter located at the upper right part of Fig. 5.4. Six discrete MOSFETs, namely IRF840 with 500V and 8A ratings, are adopted for the implementation. To avoid short circuit of the dc voltage source, a parallel circuit of resistor R49 and diode D12 are connected to the gate terminal of each MOSFET. It is seen that, due to the different time constants when the MOSFET is either turned on or turned off, one can achieve an equivalent dead time for the two MOSFETs in each arm of the inverter. Also, three current shunts of 50 $m\Omega$, namely R0, R61 and R62 are connected in series with each arm of the inverter for current sensing. In

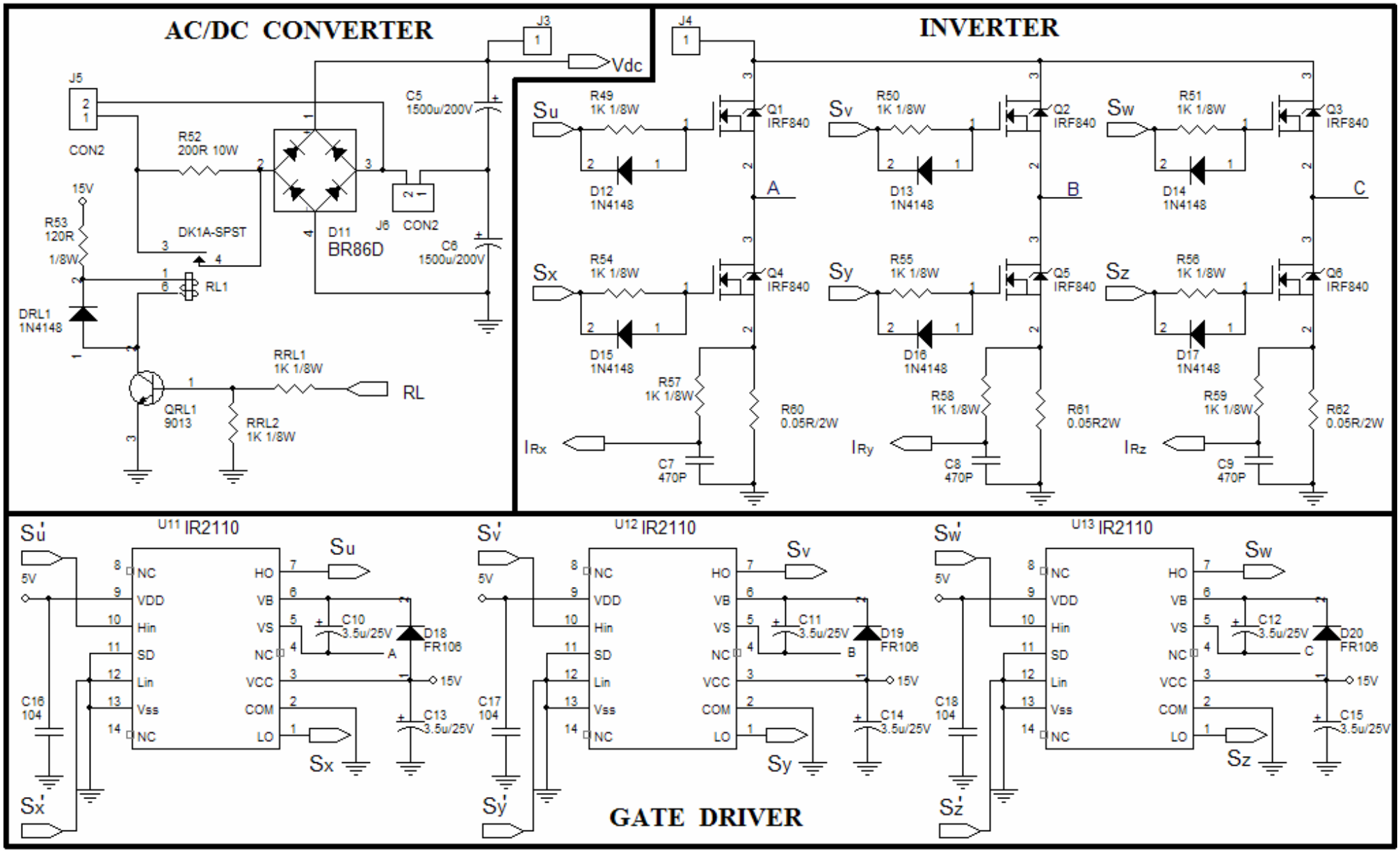


Fig. 5.4 The hardware implementation circuits of the power circuits.

addition, three low pass filters consisting of $1\,k\Omega$ resistor and $470pF$ capacitor, namely R57 and C7, R58 and C8, R59 and C9, are used to smooth out the sensed current signals. From the lower half part of Fig. 5.4, one can see that there are three gate driving ICs, namely U11, U12 and U13 implemented with IR2110, are adopted as the gate drivers for the three arms of the inverter. In addition to the previous power supply for driving the 1hp industrial blower, dc power supplies with ±15V and +5V outputs are required for the control circuits. A fly back circuit with 300V dc input and three outputs, namely ±15V and +5V, is implemented as shown in Fig. 5.5. From Fig. 5.5 one can see that an intelligent power module, namely TOP224, is adopted to simplify the circuit. Also, a photo-coupler, namely PC817, is adopted as a feedback component for input-output isolation and signal transfer. It is seen that the direct feedback control and an LC low pass filter with $3.3\,\mu H$ and $100\,\mu F$ are only applied to the major 5V output.

Next, consider the control signal circuits as follows. As described in the previous section, there contains six blocks as shown in Fig. 5.2 which in fact consists of both current controller and speed controller.

Block A : The Digital Signal Circuit

Block A of Fig. 5.2(a) basically contains the entire digital signal circuit of the proposed drive and is implemented by using a CPLD chip, namely EPM7064. A graphical editorial circuit of the selected CPLD chip output from ALTERA MAX+plus II developing

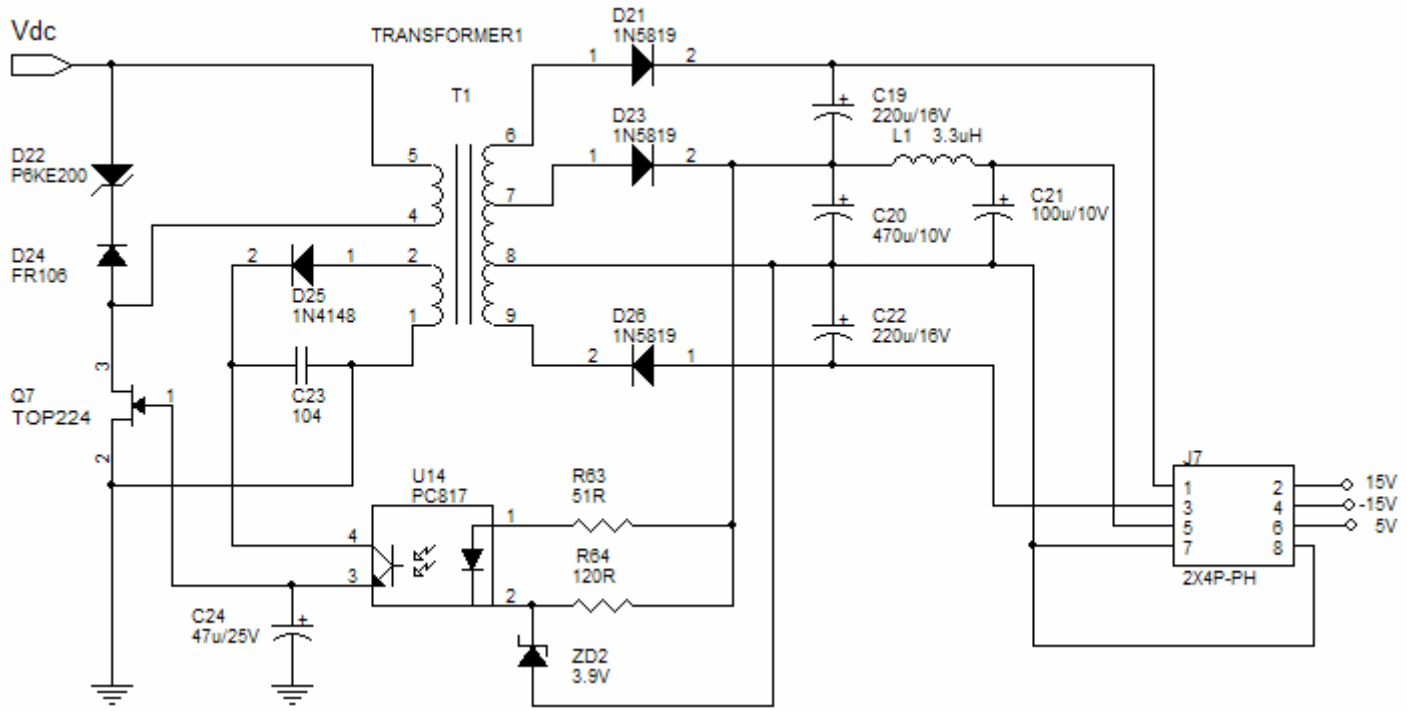


Fig. 5.5 The dc power supply circuit for control circuits.

software is shown in Fig. 5.6. From Fig. 5.6 one can see that the CPLD circuit basically contains three parts. The first part which is located at the upper left of Fig. 5.6 is the f_r pulse train signal generator for the PMBLDC motor. The three Hall-sensor signals, namely h_a, h_b and h_c, are input and controlled by V_{PWM} signal through six D-FFs and three XOR logic gates to generate the preliminary signals, namely f_a, f_b and f_c as defined in Fig. 4.2. These three signals are hen processed by an OR logic gate and a toggle flipflop to generate the desired f_r signal for later use in PLL loop control. The second part which is located at the upper right of Fig. 5.6. From Fig. 5.6 one can see that the input signal is a 6MHz clock signal and the output consists of eight digital signals, namely P0, P1,…, P7. Its main function is to serve as an 8-bit up/down counter for generating a double-slop triangular wave for PWM control use. This can be done by editing a sub-file by using the waveform editorial tool of the MAX+plus II development software. The third part is located at the lower half of Fig. 5.6. This part is in fact the implementation of the CODING TABLE OF TIMING SEQUENCE OF PHASE CURRENTS and the GATING SIGNAL GENERATOR as shown in Fig. 5.2(a). Although the coding table in Fig. 5.2(a) is decomposed into Tables 3.2 and 3.4 and the gating signal generator is illustrated by Table 3.3 for convenient explanation of the operation principle, however, they can be merged together in the final implementation as shown in Table 5.1. Thus, from Fig. 5.6 one can see that given input signals, namely h_a, h_b, h_c, C_{sign} and V_{PWM}, one can get the

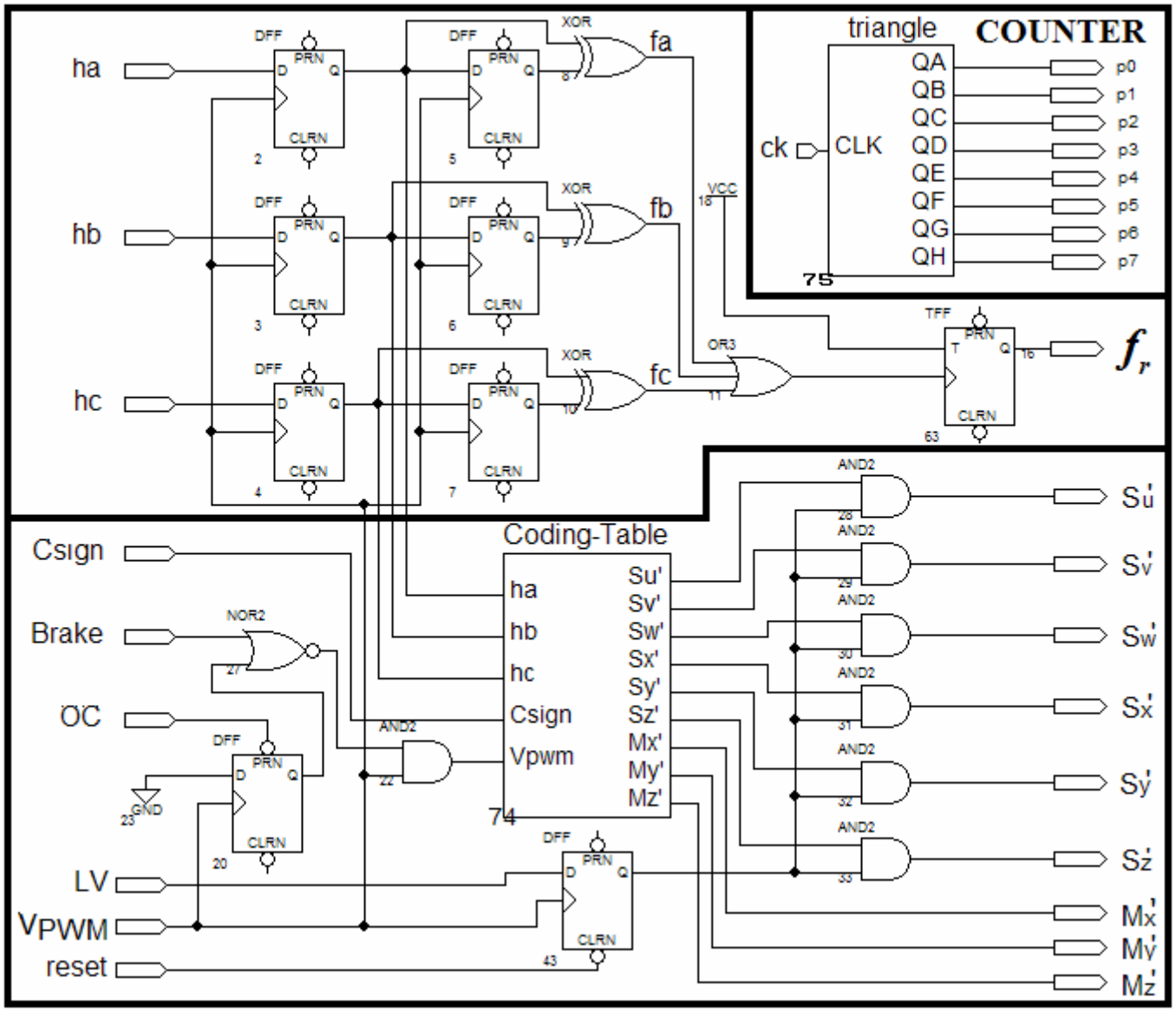


Fig. 5.6 The graphic editorial circuit of the CPLD chip EPM7064 output from ALTERA MAX+plus II developing softwar.

Table 5.1 Input/Output Signal Relation of the Coding-Table in the CPLD chip

INTERVAL	h_a	h_b	h_c	C_{sign}	V_{PWM}	Su'	Sv'	Sw'	Sx'	Sy'	Sz'	Mx'	My'	Mz'
I-A	0	0	1	0	1	1	0	0	0	1	0	0	1	0
I-F(D)	0	0	1	0	0	0	0	0	0	1	0	0	1	0
I-F(B)	0	0	1	1	0	0	0	0	0	1	0	1	0	0
I-R	0	0	1	1	1	0	0	0	0	0	0	1	0	0
II-A	1	0	1	0	1	1	0	0	0	0	1	0	0	1
II-F(D)	1	0	1	0	0	0	0	0	0	0	1	0	0	1
II-F(B)	1	0	1	1	0	0	0	0	0	0	1	1	0	0
II-R	1	0	1	1	1	0	0	0	0	0	0	1	0	0
III-A	1	0	0	0	1	0	1	0	0	0	1	0	0	1
III-F(D)	1	0	0	0	0	0	0	0	0	0	1	0	0	1
III-F(B)	1	0	0	1	0	0	0	0	0	0	1	0	1	0
III-R	1	0	0	1	1	0	0	0	0	0	0	0	1	0
IV-A	1	1	0	0	1	0	1	0	1	0	0	1	0	0
IV-F(D)	1	1	0	0	0	0	0	0	1	0	0	1	0	0
IV-F(B)	1	1	0	1	0	0	0	0	1	0	0	0	1	0
IV-R	1	1	0	1	1	0	0	0	0	0	0	0	1	0
V-A	0	1	0	0	1	0	0	1	1	0	0	1	0	0
V-F(D)	0	1	0	0	0	0	0	0	1	0	0	1	0	0
V-F(B)	0	1	0	1	0	0	0	0	1	0	0	0	0	1
V-R	0	1	0	1	1	0	0	0	0	0	0	0	0	1
VI-A	0	1	1	0	1	0	0	1	0	1	0	0	1	0
VI-F(D)	0	1	1	0	0	0	0	0	0	1	0	0	1	0
VI-F(B)	0	1	1	1	0	0	0	0	0	1	0	0	0	1
VI-R	0	1	1	1	1	0	0	0	0	0	0	0	0	1

A : representing active mode

R : representing regenerative mode

F(D) : representing freewheeling mode under driving condition

F(B) : representing freewheeling mode under braking condition

corresponding control signals such as *Su'*, *Sv'*, *Sw'*, *Sx'*, *Sy'* , *Sz'*, and *Mx'*, *My'*, *Mz'*. In addition, two inputs, namely "OC" and "Brake" as shown in Fig. 5.6 are provided for over current protection and soft stop interrupt, respectively. When the "OC" ("Brake") signal is at low (high) level, the *Vpwm* signal will be set to be at low level such that the drive operated in the freewheeling mode. Similarly, two more inputs, namely "LV" and "reset"

in Fig. 5.6 are provided for low voltage protection and state resetting respectively, when the "LV" ("reset") is at low (low) level, all the six active switch gating signals, namely *Su', Sv', Sw', Sx', Sy', Sz'* will be at low level as the initial state. In case, the motor is under running condition, then there will be no power input and the motor will be in free running condition.

Block B : The i_{eq} Synthesis Circuit

From Fig. 5.2(a) Block B one can see that by properly controlling the three transmission gates, namely *Mx', My'* and *Mz'*, one can choose the desired phase current and then share the common low pass filter. On the other hand, one can also sense three phase currents respectively at the expense of two more low pass filters to get i_{Rx}, i_{Ry} and i_{Rz} as shown in Fig. 5.4. Then, the resulting signals are amplified and taken absolute values, respectively for each phase as implemented in Section I and Section II in Fig. 5.7. From Fig. 5.7 Section III one can see that the resulting signals are then processed with a CMOS Hex voltage level shifter, namely CD4504 chip, to shift the input signals *Mx', My'* and *Mz'* from 0~5V to 0~15V to control the three bilateral switches in chip CD4066, namely *Mx, My* and *Mz* to obtain the equivalent armature current i_{eq}.

Block C : The $i_s - i_{eq}$ Signal Generator

This control signal generator circuit as shown in Fig. 5.2(a) Block C is implemented as shown in Fig. 5.8. From Fig. 5.8 it is seen that with the input current command and the

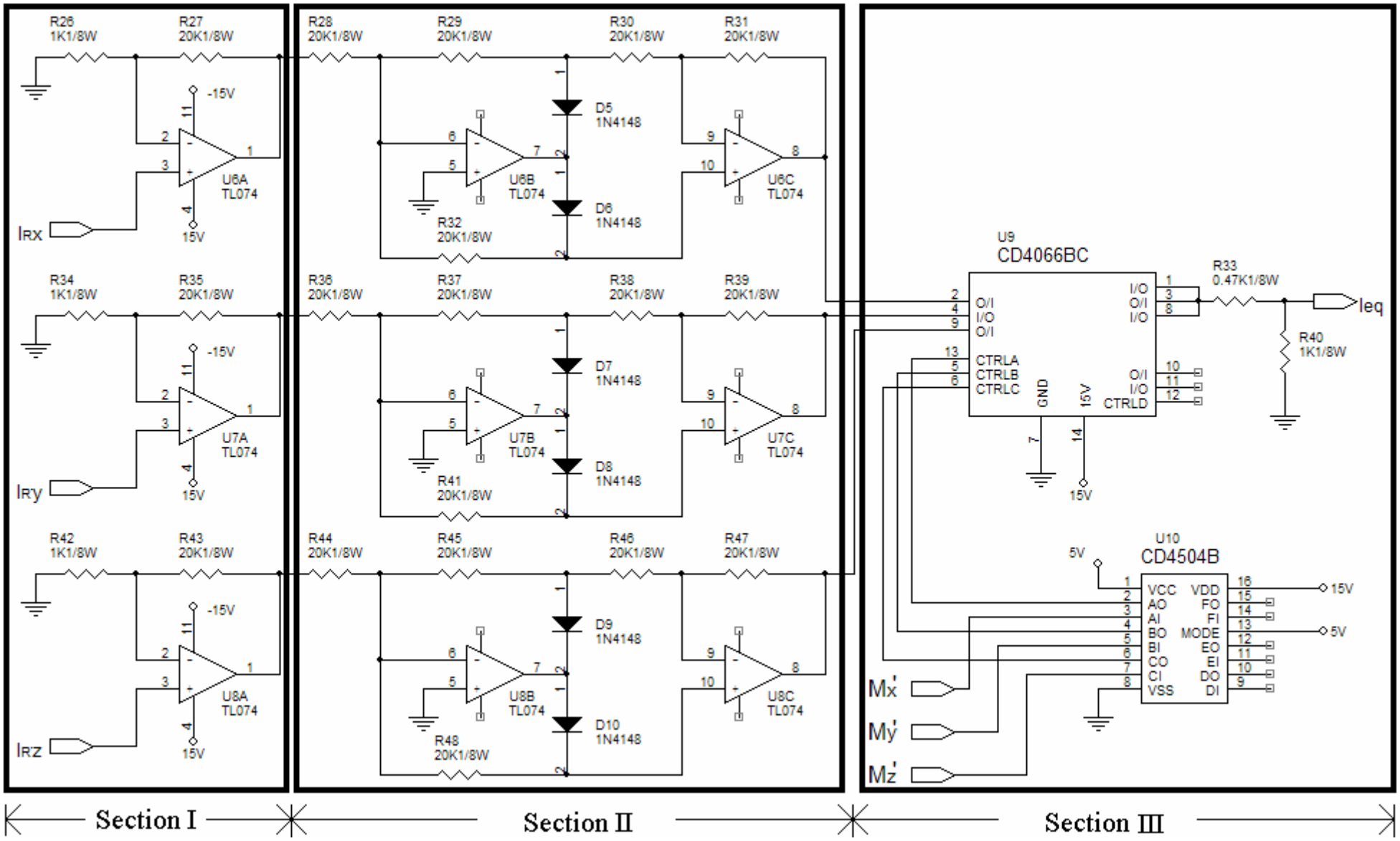


Fig. 5.7 The hardware implementation circuits of Block B in Fig. 5.2(a).

i_{eq} obtained from Fig. 5.7, the corresponding difference is first obtained through a subtractor located at lower left corner of Fig. 5.8. The resulting signal is then compared with the ground voltage to obtain the C_{sign} signal. Meanwhile, the difference signal $i_s - i_{eq}$ is sent to a PI controller together with another amplifier with magnitude gain being equal to 2. The resulting signal is then sent to an absolute circuit as marked in Fig. 5.8. Finally, the resulting signal is sent to a dc level shift circuit to shift the dc level from 0~9.2V to -9.2~9.2V.

Block D : The V_{PWM} Signal Generator

From Fig. 5.2(a) one can see that the V_{PWM} signal generator basically takes the control signal obtained from Block C and the 8-bit digital counter signals from Block A to generate the desired V_{PWM} signal. Implementation of this block is shown in Fig. 5.9. For a better understanding of the signal flow, Block A and some related circuits are also included in Fig. 5.9. From Fig. 5.9 one can see that the up/down counter 8-bit signal, namely P0, P1,…, P7, is processed by a DAC0800 chip to convert to a triangular waveform analog signal. It is then compared with the control signal obtained from Block C in Fig. 5.8 to generate the desired V_{PWM}. Also shown in Fig. 5.9 are the over current signal generator and he clock signal generator, namely “OC” and “CK” respectively for reference.

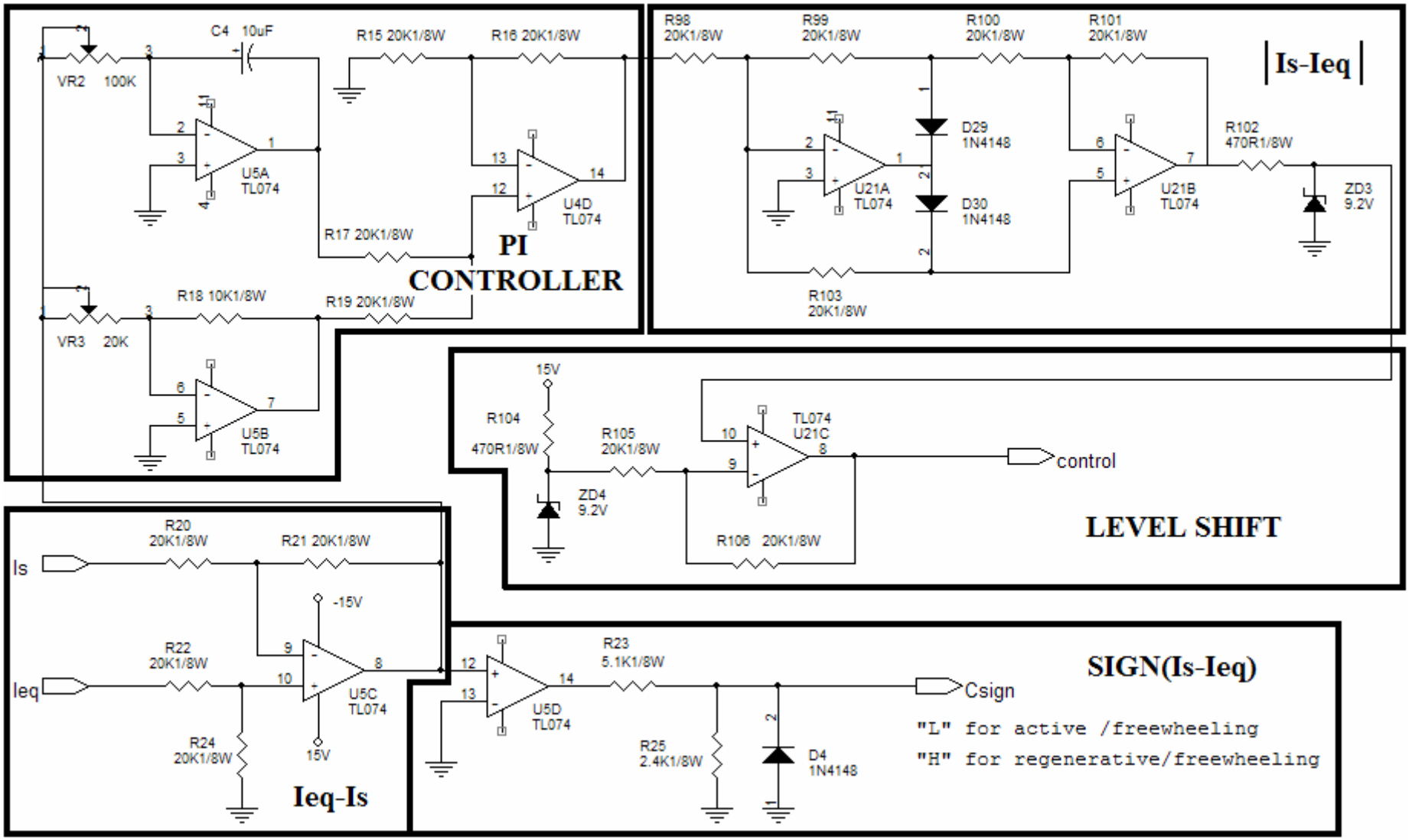


Fig. 5.8 The hardware implementation circuits of Block C in Fig. 5.2(a).

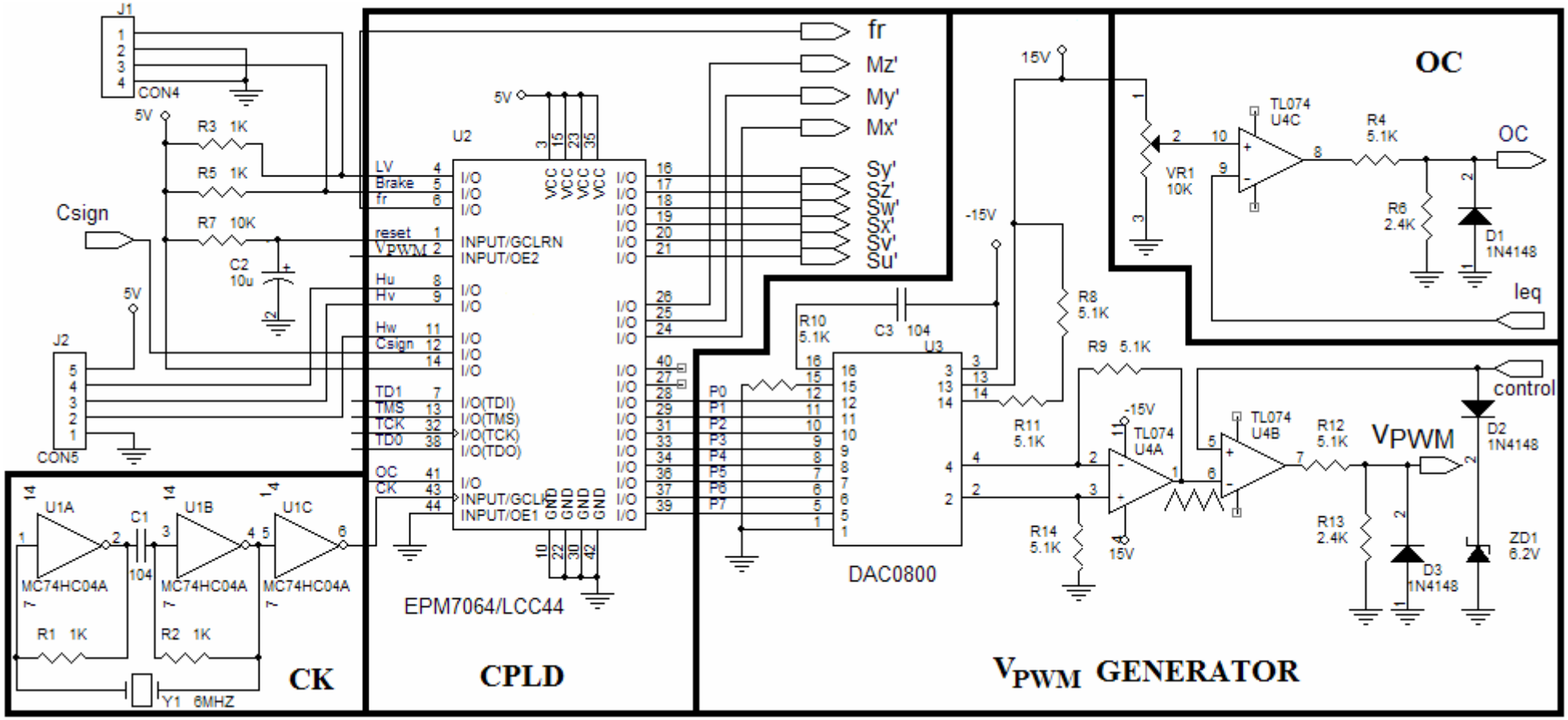


Fig. 5.9 The hardware implementation circuits of Blocks A and D in Fig. 5.2(a).

Block E : The PLL Speed Controller Circuit

From Fig. 5.2(b) one can see that the PLL speed controller is mainly used to generate the desired accurate integral signal to achieve high accuracy speed control. The corresponding implementation is shown in Fig. 5.10. From Fig. 5.10 one can see that the analog speed command signal ω_s is first processed through a circuit for VCO offset and VCO gain adjustment. It is then sent to pin 9 of PLL device, namely CD4046B, which basically includes an internal VCO and a PFD. The output signal of VCO at pin 4 of CD4046B is then connected to pin 14 to serve as one input of the PFD. The other input of the PFD, namely f_r, is connected to pin 3. Then, the output signal θ_{ep} from pin 13, which assumes one of the tri-states, namely 5V, 2.5V and 0V, is multiplied by two and then shifted to about 5V, 0V and -5V respectively. Signal θ_{ep} is then sent to a low pass filter and a voltage follower to get θ_e. Finally, the θ_e signal is then multiplied by factor *k* to get $-k\theta_e$.

Block F : The PI Speed Controller Circuit

From Fig. 5.2(b) one can see that the output signal i_s of the PI speed controller contains three components, namely the analog signals obtained from analog PI controller with k_P and (1-*k*) gains as well as analog signal $k\theta_e$ from the previous PLL speed controller. The corresponding implementation of this block is shown in Fig. 5.11. From the lower left corner of Fig. 5.11 one can see that the analog speed error ω_{er} is first obtained

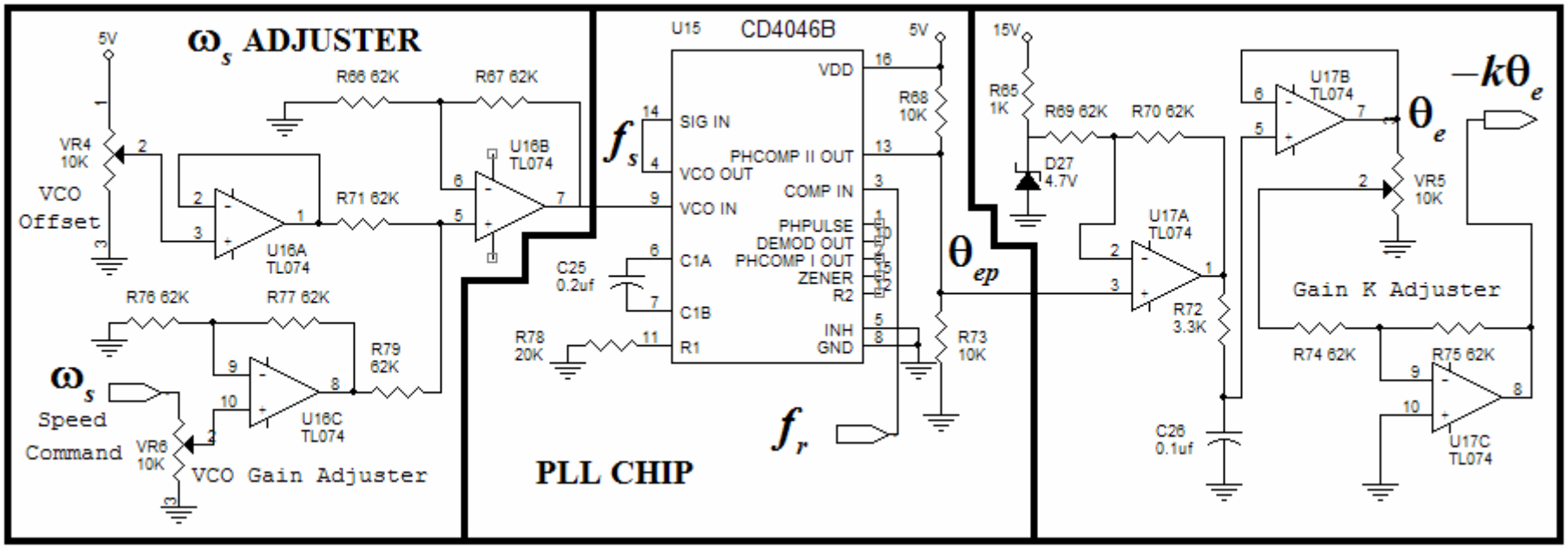


Fig. 5.10 The hardware implementation circuits of the PLL control loop of the proposed speed controller.

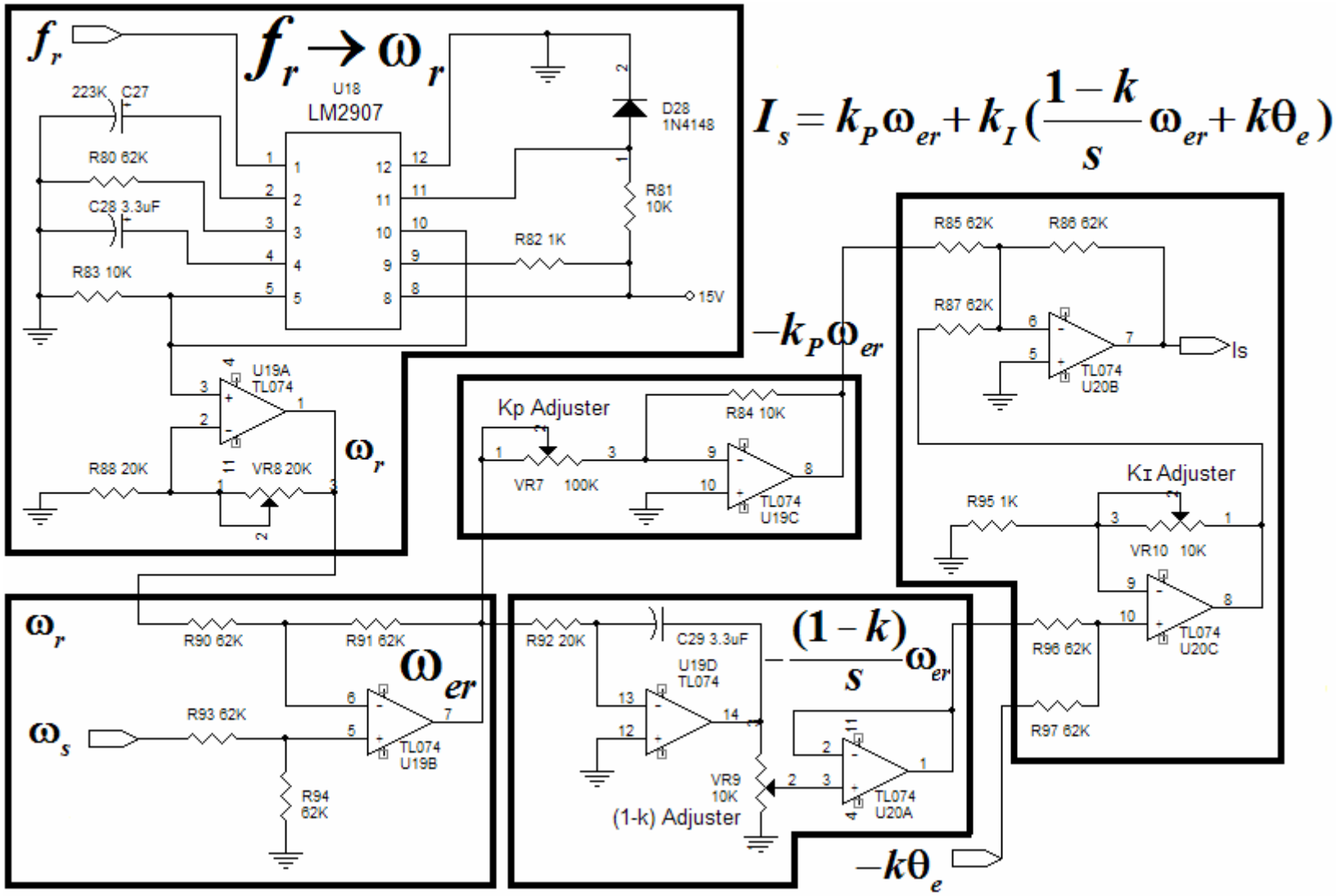


Fig. 5.11 The hardware implementation circuits of the PI control loop of the proposed speed controller.

through a subtractor. The resulting signal is then processed through a proportional controller and an integral controller with gain $-k_P$ and –(1-k) respectively as shown in Fig. 5.11. The resulting two integral signals are then added together and multiplied by scalar k_I in the k_I Adjuster circuit as shown in the lower right corner of Fig. 5.11. Finally, the corresponding signal is added with the output of the P-controller to obtain the desired i_s signal.

5.4 Simulation and Experimental Results

In order to verify the robustness and feasibility of the proposed implementation for the industrial blower system application, some experiments are tested and the experimental results are shown in Figs. 5.12-5.17. First, by applying a unit step to the PMBLDC motor plant, one can get the plant model yields

$$G_p(s) = \frac{k_s(1-\tau_L s)}{1+T_p s} = \frac{0.771(1-0.01818s)}{1+0.2s} \tag{5.1}$$

It follows that one can choose

$$G_{M^*}(s) = \frac{0.771}{1+0.2s} \tag{5.2}$$

And then choose

$$G_{IMC}(s) = G_{M^-}^{-1}(s)F(s) = \frac{1+0.2s}{0.771}\cdot\frac{1}{1+T_f s} \tag{5.3}$$

Substitute $G_P(s)$ into $G_{CA}(s) = k_P + \frac{k_I}{s}$ yields the following parameters

$$k_p = \frac{0.2}{0.771\cdot(0.01818+T_f)} \tag{5.4}$$

$$k_I = \frac{1}{0.771\cdot(0.01818+T_f)} \tag{5.5}$$

For the system to be stable then according to (4.17) T_f must be greater than $0.1818k$. Hence, if k is chosen to be 0.5 then the time constant of the low pass filter can be chosen to be 0.25sec. In that case, the corresponding phase margin is 77.6° and the gain margin is 7.86dB as shown in Fig. 5.12. Second, in order to show the effectiveness of the closed-loop current controller, the experimental results of the regulated equivalent armature current and the corresponding motor phase currents under closed-loop current control in 200rpm are shown in Fig. 5.13(a). From Fig. 5.13(a) one can see that the upper current trajectory i_{eq} is in fact synthesized from i_a, i_b and i_c of the BLDC stator currents. Since the equivalent armature current consists of six segments, each period, say the 1st interval as marked in Fig. 5.13(a) the equivalent armature current is equal to i_a and $-i_b$, and for the second interval the equivalent armature current is equal to i_a and $-i_c$, etc. Thus, from Fig. 5.13(a) one can see that the nonzero current magnitude waveforms of the equivalent armature current are quite uniform and closely tracking the

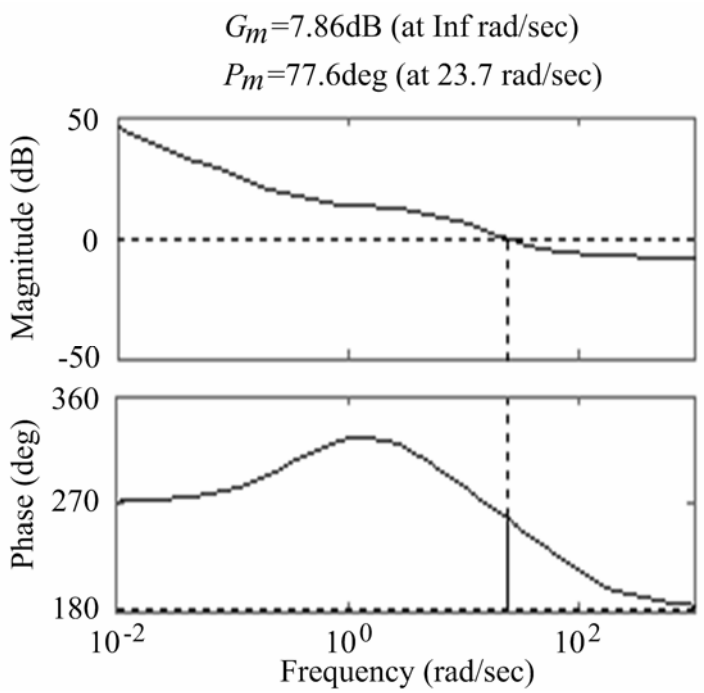
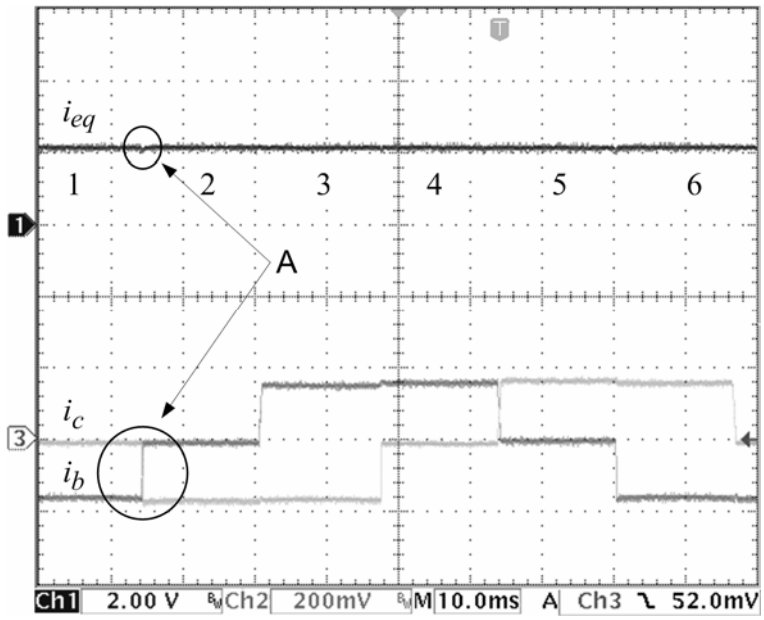
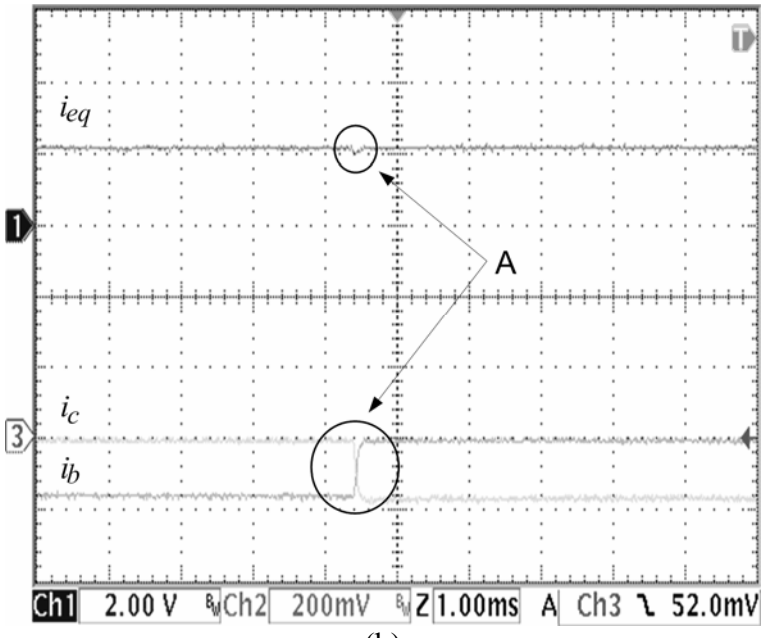


Fig. 5.12 Bode diagram of the loop gain function of the proposed controller.

constant current command. The scale of the current probe of the b-phase and c-phase curves are both 2A/div in Fig. 5.13. For clearly show the current transition between phases, portion of Fig. 5.13(a) has been expanded in Fig. 5.13(b). From Fig. 5.13(b) position A one can see that the equivalent armature current has been controlled to be nearly constant. Hence, by taking the first derivative on both sides of $i_a + i_b + i_c = 0$, one can get $|di_b / dt| \cong |di_c / dt|$ during this phase current transition interval. Therefore the commutation electromagnetic torque ripples could be suppressed. Also, the experimental results with same loading condition at 800rpm speed are shown in Fig. 5.13(c). In Fig. 5.13(c) since the operation speed of the PMBLDC motor is much higher which will induce much larger back emfs, therefore a larger commutation ripple in position B of Fig. 5.13(c) results. However from the expanded curve of Fig. 5.13(d) one can see that the commutation

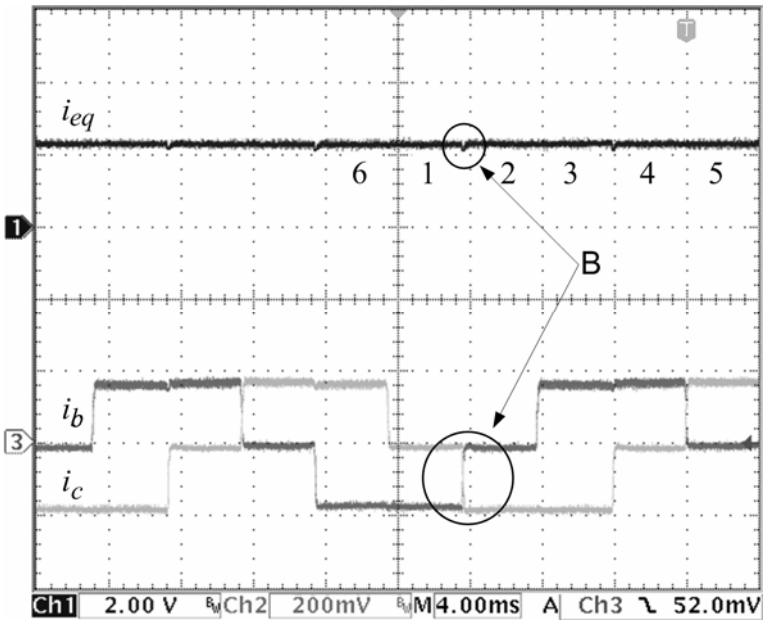


(a)

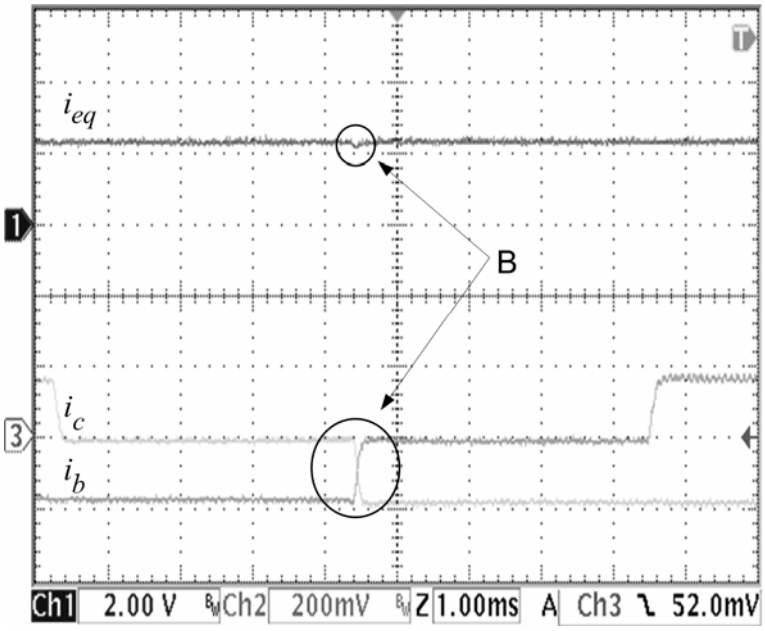


(b)

Fig. 5.13 Experimental results of the motor phase current and the equivalent armature current with equivalent armature current control. (a) At 200rpm. (b) Expanded curve of Fig. 5.13(a).



(c)



(d)

Fig. 5.13 Experimental results of the motor phase current and the equivalent armature current with equivalent armature current control. (c) At 800rpm. (d) Expanded curve of Fig. 5.13(c). (continued)

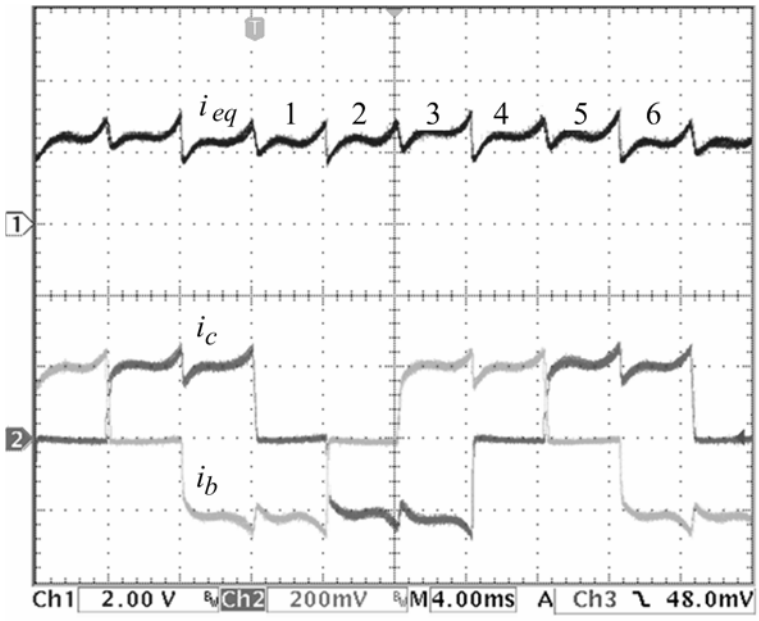
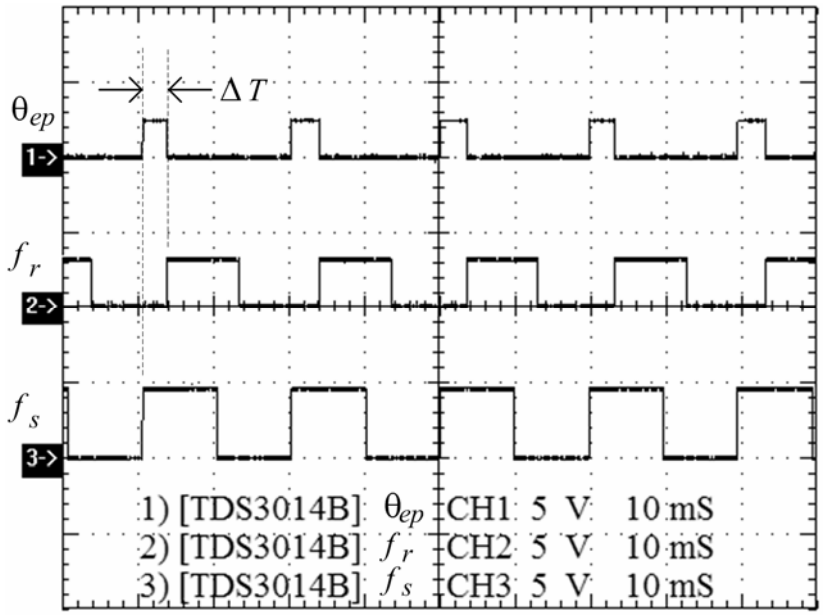


Fig. 5.14 Experimental results of the motor phase current and the equivalent armature current without equivalent armature current control.

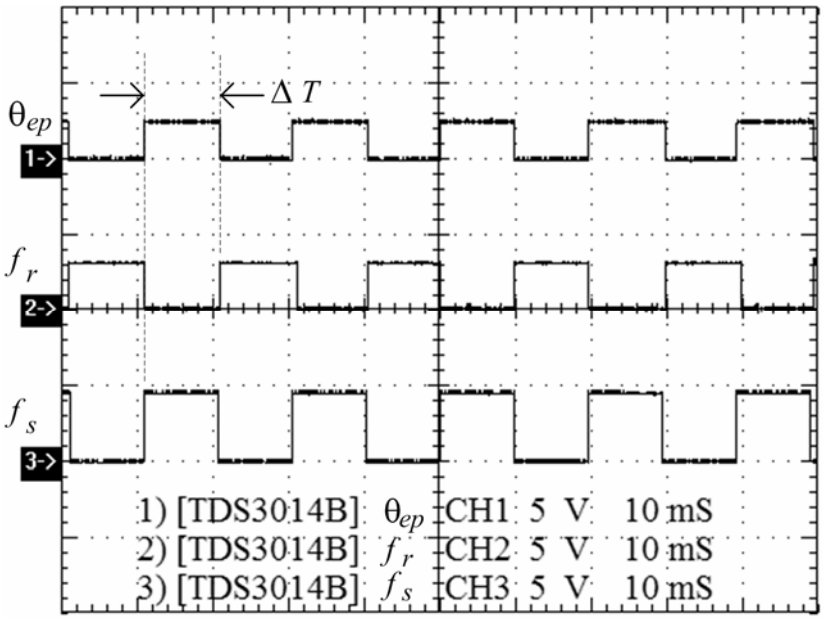
current ripple can still be regulated to be nearly constant. For comparison, under the same loading and speed conditions, the experimental results by setting the duty ratio of V_{PWM} in the open-loop current controller, which is shown in Fig. 3.8, to be 0.5 are shown in Fig. 5.14. From Fig. 5.14, one can see that, the nonzero current waveform magnitude of the equivalent armature current is still in close agreement with the phase currents, however there exists switching surges. Compared Fig. 5.13(c) and Fig. 5.14, it is worth mentioning here that with the proposed integrated current sensing technique the closed-loop control performance is greatly improved and the switching surges of the equivalent armature current can be effectively suppressed.

Third, consider the speed control of the proposed drive system at 333rpm corresponding to no load, 5Nt-m load and 9Nt-m load conditions, respectively. The corresponding waveforms of phase differences pulse train signal, θ_{ep}, the command pulse train signal f_s and the motor speed pulse train signal f_r are shown in Fig. 5.15. From Fig. 5.15 one can see that the phase error pulse train signal θ_{ep} is changed from 0V to 2.5V while f_s changes from low to high state and change state from 2.5V to 0V while f_r changes from low to high state. Moreover, the duty ratio ΔT of θ_{ep} increases with the increasing load as can be seen from Fig. 5.15. It is seen that under steady state the motor speed pulse train (f_r) can indeed track the command speed pulse train (f_s) without speed error.

Fourth, consider the transient experimental results as shown in Fig. 5.16. In Fig. 5.16 the drive system is originally operated at f_r at 22Hz under 4 Nt-m load torque. Then at $t = A$, the speed command f_s is increased with a step change from 22 Hz to 93 Hz. Then, at $t = B$ the 4 Nt-m load is removed suddenly for some period times and then added again at $t = C$. The corresponding *a*-phase current, ω_r and f_r trajectories in Fig. 5.16 show that even under transient conditions, the proposed drive system can provide rather smooth responses electrically and mechanically. For better view, Fig. 5.16(b) shows the amplified portion of part of Fig. 5.16(a) for reference. From Fig. 5.16(b) one can indeed see the nice control performance of the proposed PLL assisted IMC. Finally, the power consumption

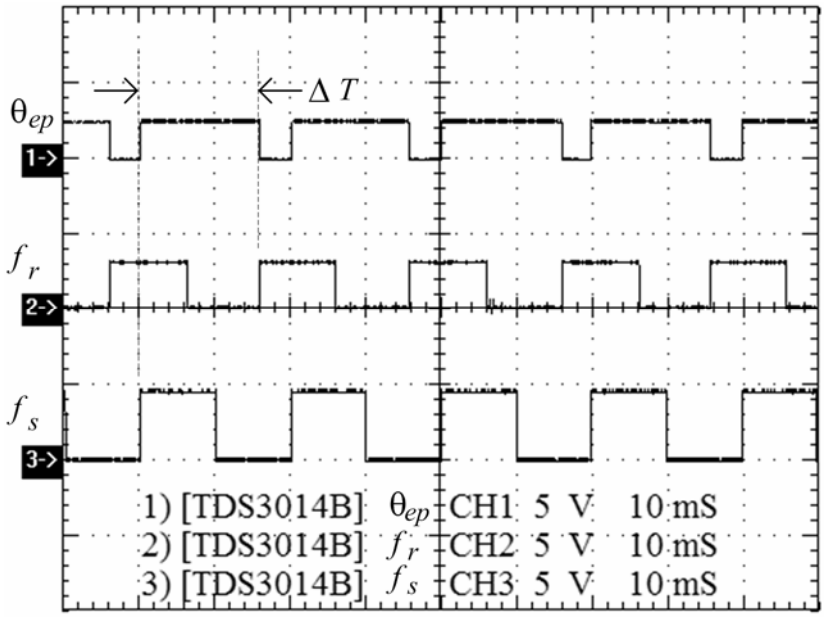


(a)



(b)

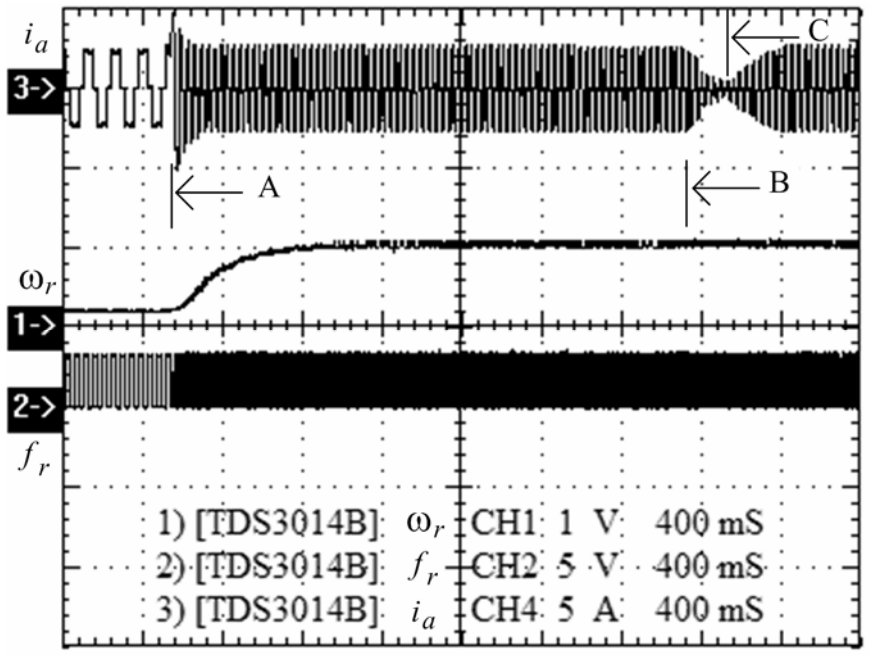
Fig. 5.15 Waveforms of f_s, f_r and θ_{ep} of the proposed drive while the motor is operated at 333rpm and with different load conditions. (a) No load. (b) 5Nt-m load.



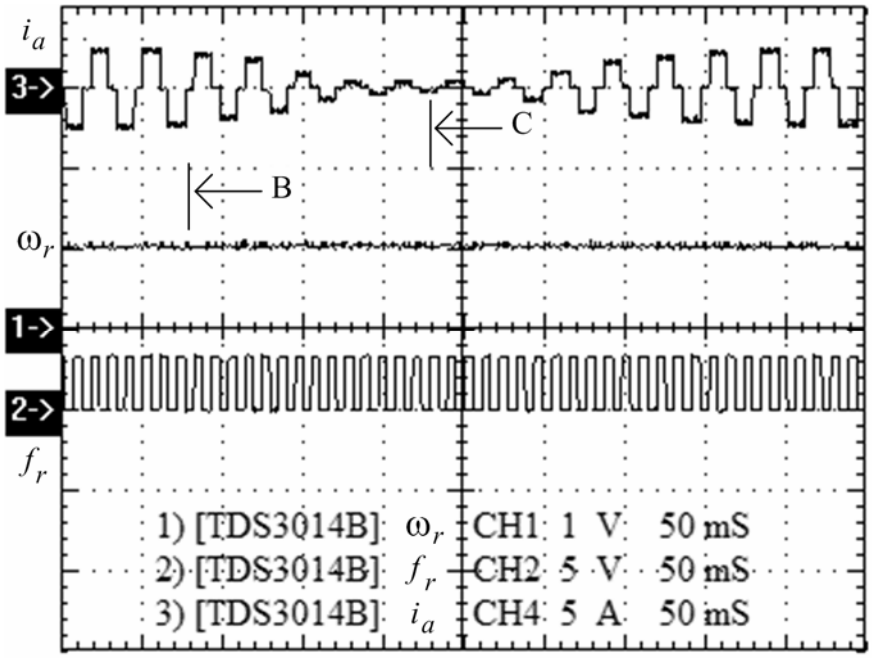
(c)

Fig. 5.15 Waveforms of f_s, f_r and θ_{ep} of the proposed drive while the motor is operated at 333rpm and with different load conditions. (c) 9Nt-m load. (continued)

comparison between the original industrial blower system driven by a traditional three-phase induction motor system and that driven by the proposed control system is shown in Fig. 5.17(a). The speed and power ratings of the three-phase induction motor are 1100rpm and 850W, and that of the self-designed PMBLDC motor are 1100rpm and 746W respectively. Besides, the resistance of the shunt resistors Rx, Ry and Rz in Fig. 5.8 is 0.05Ω and the power consumption of them is less than 1W respectively in the proposed industrial blower system. The corresponding pictures of the two motors are shown in Fig. 5.17(b). The weights of these two testing motors are 10.5 kg and 4.5 kg individually. From

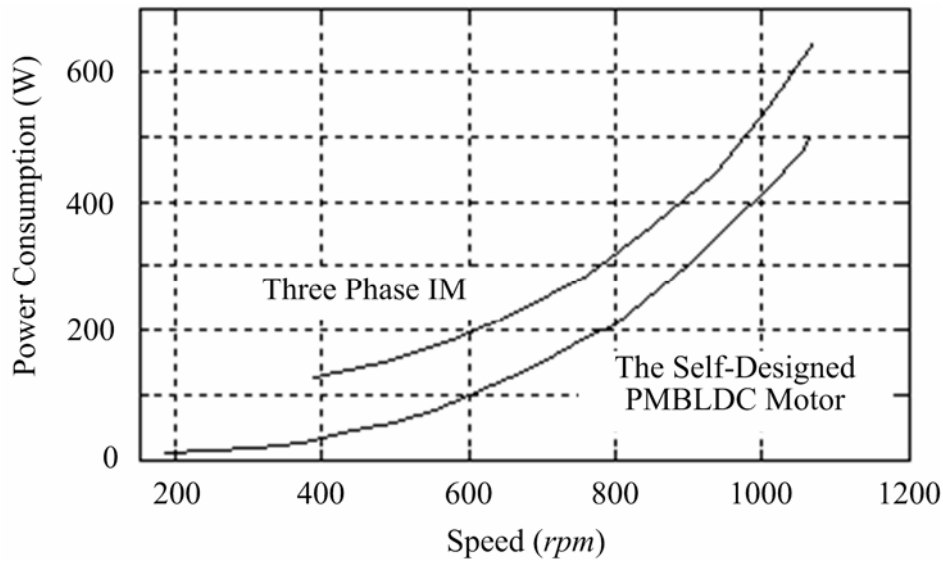


(a)

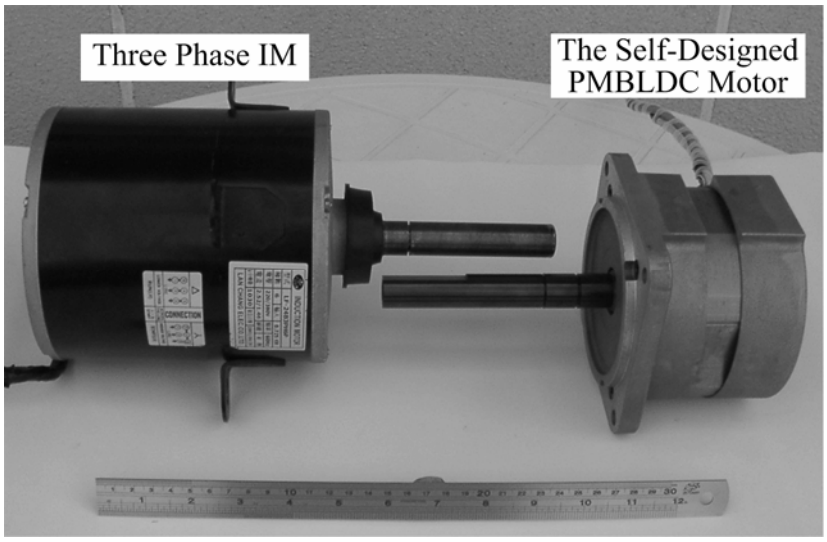


(b)

Fig. 5.16 Transient experimental results of the proposed drive. (a) Waveforms of the *a*-phase current, ω_r and f_r. (b) The corresponding amplified portion of part of (a).



(a)



(b)

Fig. 5.17 Comparison of the three-phase induction motor and the self-designed PMBLDC motor of the industrial blower. (a) Comparison of the power consumption. (b) Comparison of the volume.

Fig. 5.17(a) and Fig. 5.17(b), one can see that the proposed drive system can save the blower system power consumption by 20% at rated speed, 60% at 550rpm and more than 80% at 380rpm, as well reduce the total volume and weight by 30% and 57% respectively.