# 摘　要

內嵌式永磁同步電動機以其具有高效率、高功率密度、高轉矩慣量比以及寬廣之轉速操作範圍，因此在產業界之應用愈來愈廣，本論文之主要目的即在探討如何利用通訊領域常用之鎖相迴路控制技術，以設計一適合交流電動機應用之可調速精密速度控制器。

基本上本論文之主要貢獻可分為下列三點說明之。首先，針對具轉動慣量特性之電動機提出一新型相位頻率偵測器(Phase Frequency Detector, PFD)，其輸出視轉速差很大、稍大於零及等於零時，分別設定為零、線性虛擬相位差及真實相位差，可使全速調整範圍獲得良好的協調關係。第二，基於前述 PFD，提出一新型可調式精密速度控制器；其特點是不僅採用單位安培最大轉矩控制策略以獲得快速響應之效果，並且可達更精準之速率控制精度，其架構則包含雙迴路控制，第一迴路即為一般產業界常採用之 PI 控制器，而另一迴路則為基於前述 PFD 之鎖相迴路之控制，可獲得更佳鎖相控制強韌性。此外，文中並就所提新型精密速度控制器之設計提出一些準則，俾快速滿足控制器規格。第三點，本論文最後並以德州儀器公司推出的 DSP TMS320F2812 結合 FPGA LFEC10E 實現新型鎖相迴路速度控制器之控制法則，實際針對一 6 極 2 馬力之內嵌式永磁電動機製作一硬體電路雛型來驗證本論文所提控制策略之可行性。經實驗結果驗證，此新型鎖相迴路控制器在轉速從 482 rpm 至 3122 rpm 均可獲得鎖相控制之效果。

關鍵字：內嵌式永磁同步電動機，鎖相迴路，數位訊號處理器，現場可程式化邏輯閘陣列。

# Abstract

Due to the merits of high efficiency, high power density, high torque to inertia ratio and wide speed range, interior permanent magnet (IPM) motors have now attracted more and more industrial applications. The objective of this thesis is to design a more precise speed controller for AC motors by using phase-locked loop (PLL) technique, which is a common technique used in communication systems.

Basically, the major contributions of this thesis may be summarized as follows. First, considering the inherent inertia, a novel phase frequency detector (PFD) is proposed. Depending on whether the magnitude of the speed error is large, small, or almost zero, the output of the proposed PFD is set equal to zero, linear virtual phase difference, real phase error, respectively. By this way, the generated control torque components due to speed error and phase error can be properly coordinated during the whole speed range. Second, based on the proposed PFD, a novel precise adjustable speed controller is proposed. Special merits include adopting the maximum torque per ampere control strategy to achieve fast dynamic response and being able to achieve much better accuracy. Basically, the proposed speed controller configuration comprises two control loops. One is the conventional PI speed control loop as is used in common industry and the other is the previously mentioned PFD PLL loop to achieve more robust PLL control. In addition, some design criteria are presented for fast design of the proposed controller to satisfy the specification. Third, a prototype system is constructed for a 6-pole 2-hp IPM motor based on the proposed controller by using DSP

TMS320F2812 together with FPGA LFEC10E to verify the validity of the proposed controller. Experimental results of the prototype show that the corresponding IPM motor can be controlled smoothly from 482 rpm to 3122 rpm with zero speed error.

*Keywords:* Interior permanent magnet synchronous motors, Phase-locked loop, Digital signal processor, Field-programmable gate array.