CHAPTER III

THE PROPOSED SWITCHING FLOW-GRAPH MODELING TECHNIQUE FOR THREE-PHASE INVERTERS [42]

3.1 The Concept of Virtual Switch For Inverters

Consider a typical three-phase PWM inverter as shown in Fig. 3.1 where S_{jP}, S_{jN} and D_{jP}, D_{jN}, $j \in \{A, B, C\}$ represent controllable switches and diodes respectively and a three-phase RL impedance load is connected as an example.

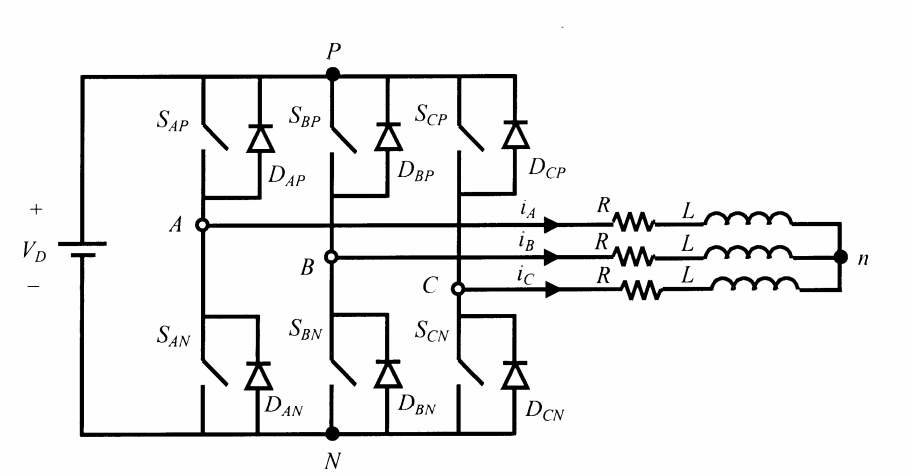


Fig. 3.1 The circuit configuration of the PWM inverter.

According to the basic operating principle of the inverter, it is required that 1) for any time, switch S_{jP} and S_{jN}, $j \in \{A, B, C\}$ should not be ON simultaneously to avoid short circuit of the DC source; 2) for any time, it is not allowed to result in an open circuit for any phase. For convenient explanation of the virtual switch concept, first choose the A-phase leg of Fig. 3.1 as an example. There are two controllable switches, namely S_{AP} and S_{AN}, and two diodes, namely D_{AP} and D_{AN}. Therefore, there are sixteen switching states according to the combination of ON/OFF

states of each switch and each diode. Nevertheless, only six switching states as described in Table 3.1 are qualified for the inverter control.

Table 3.1 Six qualified switching states

Value of v_{AN}	*State Number*	*Switching States ($S_{AP}, D_{AP}, S_{AN}, D_{AN}$)*
$v_{AN} = V_D$	*State 1*	*(OFF, ON, OFF, OFF)*
	State 2	*(ON, OFF, OFF, OFF)*
	State 3	*(ON, ON, OFF, OFF)*
$v_{AN} = 0$	*State 4*	*(OFF, OFF, OFF, ON)*
	State 5	*(OFF, OFF, ON, OFF)*
	State 6	*(OFF, OFF, ON, ON)*

From Table 3.1 one can see that states 2, 4 and 6 only occur for $i_A > 0$ and states 1, 3, and 5 occur for $i_A < 0$. Also, the value of v_{AN} equals to V_D for states 1, 2 and 3 and zero for states 4, 5, and 6.

Similar to [32] for the controllable switches of Fig. 3.1 one can define the following switching functions:

$$F_{S_{jk}}(t) = \begin{cases} 1 & , \text{ when } S_{jk} \text{ is } ON \\ 0 & , \text{ when } S_{jk} \text{ is } OFF \end{cases} \tag{3.1}$$

$$\overline{F_{S_{jk}}}(t) = \begin{cases} 1 & , \text{ when } S_{jk} \text{ is } OFF \\ 0 & , \text{ when } S_{jk} \text{ is } ON \end{cases} \tag{3.2}$$

$$j \in \{A, B, C\}, \quad k \in \{P, N\}$$

Although D_{AP} and D_{AN} are uncontrollable, in order to obtain simple switching flow-graph which can deal with different voltage polarities, it is necessary to define its corresponding switching functions. From the previous inverter operation constraints, one can find the following conditions for diodes:

If $[(S_{AN}$ *is* $OFF)$ *AND* $(i_A(t) < 0)]$ *is true, then* D_{AP} *is* ON; *otherwise,* D_{AP} *is* OFF.

If $[(S_{AP}$ *is* $OFF)$ *AND* $(i_A(t) > 0)]$ *is true, then* D_{AN} *is* ON; *otherwise,* D_{AN} *is* OFF.

It follows that the corresponding switching functions can now be defined as:

$$F_{D_{AP}}(t) \overset{\Delta}{=} \begin{cases} 1 & , \quad when \quad D_{AP} \quad is \quad ON \\ 0 & , \quad when \quad D_{AP} \quad is \quad OFF \end{cases} \tag{3.3}$$

$$F_{D_{AN}}(t) \overset{\Delta}{=} \begin{cases} 1 & , \quad when \quad D_{AN} \quad is \quad ON \\ 0 & , \quad when \quad D_{AN} \quad is \quad OFF \end{cases} \tag{3.4}$$

Further observation of the previous conditions reveals that

$$F_{D_{AP}}(t) = \overline{F_{S_{AN}}}(t) \quad AND \quad (sign(-i_A)) \tag{3.5}$$

$$F_{D_{AN}}(t) = \overline{F_{S_{AP}}}(t) \quad AND \quad (sign(i_A)) \tag{3.6}$$

$$sign(x) \overset{\Delta}{=} \begin{cases} 1, & x > 0 \\ 0, & x < 0 \end{cases} \tag{3.7}$$

Thus, based on the previous definitions one can now define the virtual switch S_A for leg A in Fig. 1 with the following operation condition:

If $\{ [(S_{AP} \ is \ ON) \ AND \ (i_A > 0)] \ OR \ (D_{AP} \ is \ ON) \}$ *is true, then* S_A *is ON; otherwise,* S_A *is OFF.*

Also, the corresponding virtual switching functions, $F_A(t)$ and $\overline{F_A}(t)$ are defined as:

$$F_A(t) \overset{\Delta}{=} \begin{cases} 1 & , \quad when \quad S_A \quad is \quad ON \\ 0 & , \quad when \quad S_A \quad is \quad OFF \end{cases} \tag{3.8}$$

$$\overline{F_A}(t) \overset{\Delta}{=} \begin{cases} 1 & , \quad when \quad S_A \quad is \quad OFF \\ 0 & , \quad when \quad S_A \quad is \quad ON \end{cases} \tag{3.9}$$

It is also straightforward to see that

$$F_A(t) = [F_{S_{AP}}(t) \quad AND \quad (sign(i_A))] \quad OR \quad (F_{D_{AP}}(t)) \tag{3.10}$$

$$\overline{F_A}(t) = [F_{S_{AN}}(t) \quad AND \quad (sign(-i_A))] \quad OR \quad (F_{D_{AN}}(t)) \tag{3.11}$$

$$F_A(t) + \overline{F_A}(t) = 1 \tag{3.12}$$

From the above definitions of (3.8) and (3.9) as well (3.12) one can see that the characteristics of the virtual switch S_A and its corresponding switching functions

$F_A(t)$ and $\overline{F_A}(t)$ are the same as that of [32] for DC converters.

In summary, for the inverter of Fig. 3.1, the operation condition of D_{jP} and D_{jN} can be represented as:

$$\begin{aligned}&If\ \left[\left(S_{jN}\ \ is\ \ OFF\right)\ \ AND\ \ \left(i_j(t)<0\right)\right]\ \ is\ \ true,\\&then\ \ D_{jP}\ \ is\ \ ON;\ \ otherwise,\ \ D_{jP}\ \ is\ \ OFF.\end{aligned}$$

$$\begin{aligned}&If\ \left[\left(S_{jP}\ \ is\ \ OFF\right)\ \ AND\ \ \left(i_j(t)>0\right)\right]\ \ is\ \ true,\\&then\ \ D_{jN}\ \ is\ \ ON;\ \ otherwise,\ \ D_{jN}\ \ is\ \ OFF.\\&j\in\{A,B,C\}\end{aligned}$$

Also, the corresponding switching functions are defined as:

$$\begin{aligned}F_{D_{jP}}(t)&\overset{\Delta}{=}\begin{cases}1 & ,\quad when\ \ D_{jP}\ \ is\ \ ON\\0 & ,\quad when\ \ D_{jP}\ \ is\ \ OFF\end{cases}\\&=\overline{F_{S_{jN}}}(t)\ \ AND\ \ \left(sign\left(-i_j\right)\right)\end{aligned}\tag{3.13}$$

$$\begin{aligned}F_{D_{jN}}(t)&\overset{\Delta}{=}\begin{cases}1 & ,\quad when\ \ D_{jN}\ \ is\ \ ON\\0 & ,\quad when\ \ D_{jN}\ \ is\ \ OFF\end{cases}\\&=\overline{F_{S_{jP}}}(t)\ \ AND\ \ \left(sign\left(i_j\right)\right)\end{aligned}\tag{3.14}$$

$$sign(x)\overset{\Delta}{=}\begin{cases}1, & x>0\\0, & x<0\end{cases}\tag{3.15}$$

Therefore, the operation condition of the virtual switch S_j can be defined as:

$$\begin{aligned}&If\ \ \left\{\ \left[\left(S_{jP}\ \ is\ \ ON\right)\ \ AND\ \ \left(i_j>0\right)\right]\ \ OR\ \ \left(D_{jP}\ \ is\ \ ON\right)\ \right\}\ \ is\ \ true,\\&then\ \ S_j\ \ is\ \ ON;\ \ otherwise,\ \ S_j\ \ is\ \ OFF.\\&\quad j\in\{A,B,C\}\end{aligned}$$

Also, the corresponding switching functions $F_j(t)$ and $\overline{F_j}(t)$ of S_j are defined as:

$$\begin{aligned}F_j(t)&\overset{\Delta}{=}\begin{cases}1 & ,\quad when\ \ S_j\ \ is\ \ ON\\0 & ,\quad when\ \ S_j\ \ is\ \ OFF\end{cases}\\&=\left[F_{S_{jP}}(t)\ \ AND\ \ \left(sign\left(i_j\right)\right)\right]\ \ OR\ \ \left(F_{D_{jP}}(t)\right)\end{aligned}\tag{3.16}$$

$$\overline{F_j}(t) \triangleq \begin{cases} 1 & , \quad when \quad S_j \quad is \quad OFF \\ 0 & , \quad when \quad S_j \quad is \quad ON \end{cases}$$
$$= \left[F_{S_{jN}}(t) \quad AND \quad \left(sign\left(-i_j\right)\right)\right] \quad OR \quad \left(F_{D_{jN}}(t)\right) \tag{3.17}$$

$$F_j(t) + \overline{F_j}(t) = 1 \tag{3.18}$$
$$j \in \{A, B, C\}$$

By introducing the above virtual switches, it is found that one can obtain the following equivalent circuit as shown in Fig. 3.2. The virtual switch S_j can be represented as a SPDT (single-pole double-throw) switch.

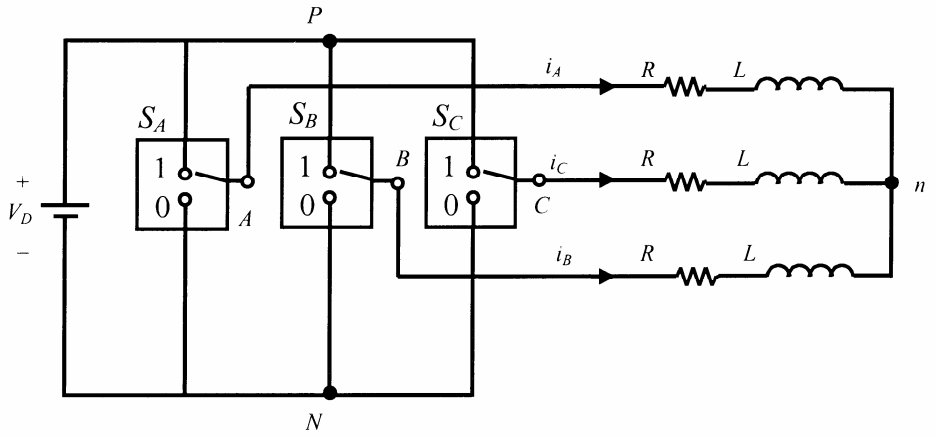


Fig. 3.2 Equivalent circuit of Fig. 3.1.

3.2 The Proposed Switching Flow-Graph for Three-Phase Inverters

From Fig. 3.2 one can see that for $j \in \{A, B, C\}$, when S_j is ON, v_{jN} equals to V_D, otherwise, v_{jN} equals to zero. According to the equivalent circuit one can write the following KVL equations.

$$v_{jN} = Ri_j(t) + L\frac{di_j(t)}{dt} + v_{nN}(t) \tag{3.19}$$
$$j \in \{A, B, C\}$$

Hence, when S_j is ON, one can obtain

$$V_D = Ri_j(t) + L\frac{di_j(t)}{dt} + v_{nN}(t) \tag{3.20}$$

and when S_j is OFF

$$0 = Ri_j(t) + L\frac{di_j(t)}{dt} + v_{nN}(t) \tag{3.21}$$

From Fig. 3.2, one can obtain

$$\begin{aligned} v_{jn}(t) &= Ri_j(t) + L\frac{di_j(t)}{dt} \\ &= (R + pL)i_j(t) \end{aligned} \tag{3.22}$$

where p operator represents the time differentiation. Now by choosing V_D, v_{jN}, v_{jn}, v_{nN}, and i_j, $j \in \{A, B, C\}$, as nodal variables, one can draw the flow-graphs G_{j_ON} and G_{j_OFF} corresponding to S_j ON and OFF as shown in Fig. 3.3(a) and 3.3b, respectively.

From Fig. 3.3c one can see that by using a switching branch with virtual switching function $F_j(t)$, one can combine two flow-graphs corresponding to S_j is ON and S_j is OFF respectively in exactly the same form as that of [32]. Furthermore, for completeness, one can draw, according to equation (3.16), the virtual switching function $F_j(t)$ of virtual switch S_j as shown in Fig. 3.3(d). From Fig. 3.3 it is seen that three switching flow-graphs corresponding to A, B, and C phases respectively seem entirely decoupled. Further examination reveals that they are, in fact, coupled together through v_{nN}. From equation (3.19) and $i_A + i_B + i_C = 0$ one can obtain

$$v_{nN}(t) = \tfrac{1}{3}(v_{AN} + v_{BN} + v_{CN}) \tag{3.23}$$

It follows from (3.23) and Fig. 3.3 that the final switching flow-graph model of the three-phase inverter can be drawn as show in Fig. 3.4.

From Fig. 3.4 one can see that, by using the proposed virtual switch concept to obviate the trouble of considering different voltage polarities, one can get a very simple switching flow-graph model of the inverter as compared with [36]. In addition, the corresponding virtual switching functions can also be obtained very simply through simple logic operations as shown in Fig. 3.3(d). From Fig. 3.4 one can see

that the sub-circuit of each arm (phase) of the full-bridge inverter is almost decoupled from other two arms (phases) except for two nodal variables, namely v_{jN} and v_{jn}. Fourth, from Fig. 3.3(d) one can also observe that the corresponding switching functions, namely $F_{D_{jP}}(t)$, of diodes are also available simultaneously while getting $F_j(t)$. With this information, it is possible to make this model more flexible in different applications such as considering the dead-time effect of active switches. Finally, it is worth pointing out here that, in the proposed switching flow-graph model, it is not necessary to use $\overline{F_j}(t)$ and $F_{D_{jN}}(t)$ functions.

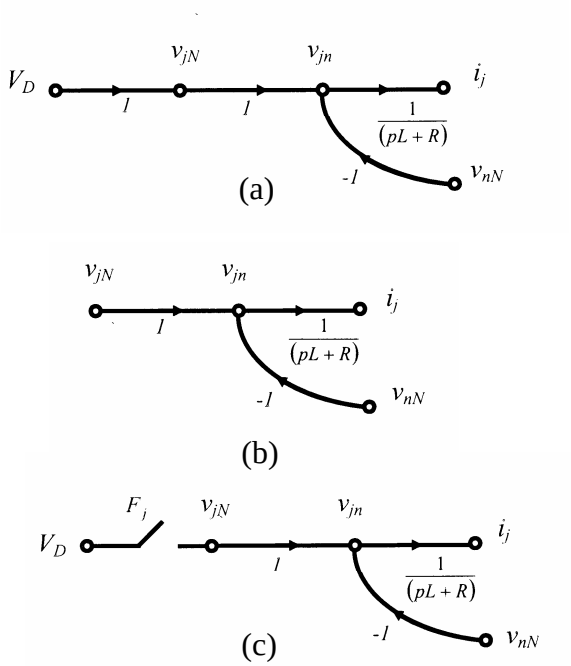


Fig. 3.3 Switching flow-graph for j phase, $j \in \{A, B, C\}$ (a) when S_j is ON (b) when S_j is OFF (c) combined flow-graph using the switching branch (d) the corresponding virtual switching function.

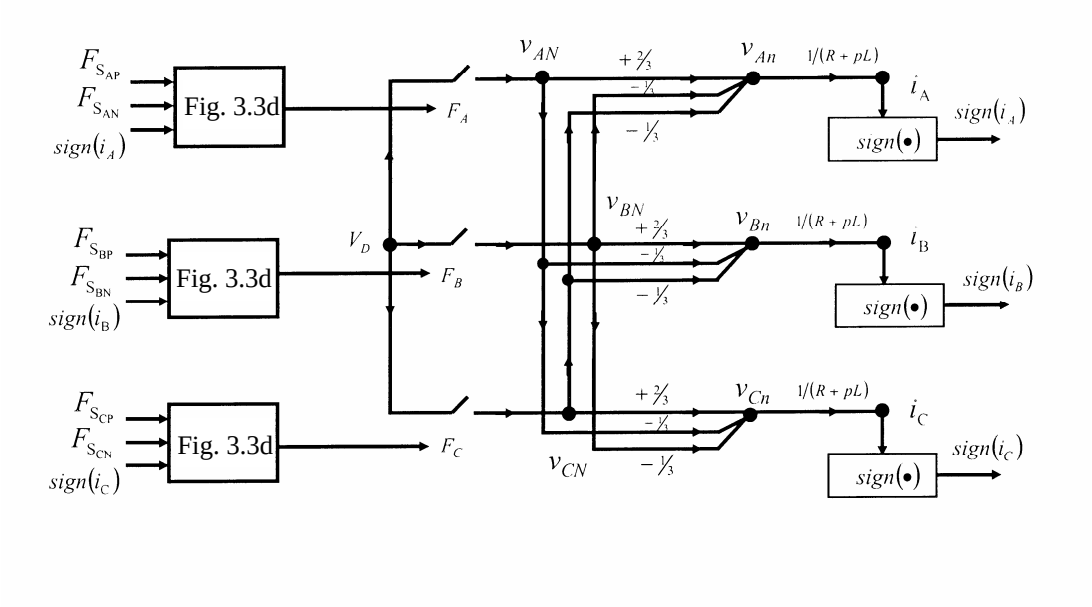


Fig. 3.4 The proposed switching flow-graph model for three-phase PWM inverters.

3.3 The Corresponding Models Derived from Switching Flow-Graph Model

Once the switching flow-graph is obtained one can follow a similar procedure as [32]-[35] to obtain the corresponding large-signal, steady state, and small-signal models, respectively.

A. Large-signal model

From Fig. 3.4, one can see that when virtual switching function $F_j(t)$ equals to one, then v_{jN} equals to V_D; otherwise, v_{jN} equals to zero. Therefore, the relationship between v_{jN} and V_D can be described as

$$v_{jN}(t) = V_D F_j(t) \quad , j \in \{A, B, C\} \tag{3.24}$$

According to equation (3.24), the large-signal model can be obtained by replacing the switching branches with multipliers as shown in Fig. 3.5

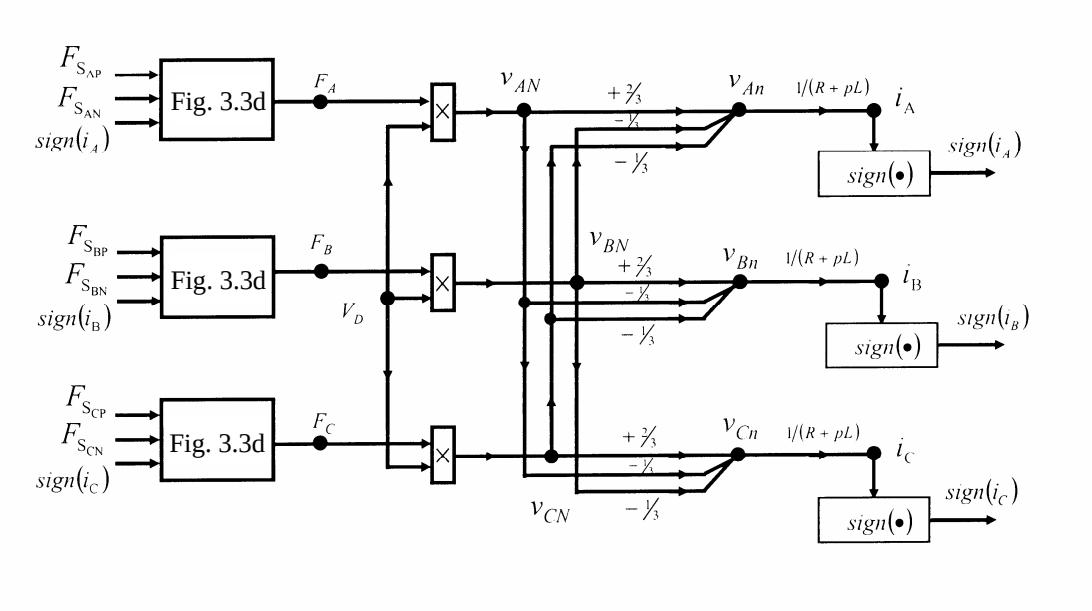


Fig. 3.5 The large-signal model derived from Fig. 3.4.

B. Steady state Model

Similarly, one can use the well known state-space averaging technique [1] to obtain the corresponding steady state model. First, let $F_{S_{jP}}{}^{*}(t)$, $F_{S_{jN}}{}^{*}(t)$, $F_j{}^{*}(t)$ and $i_j{}^{*}(t)$, $j \in \{A,B,C\}$, represent the corresponding steady state signals of $F_{S_{jP}}(t)$, $F_{S_{jN}}(t)$, $F_j(t)$ and $i_j(t)$ respectively. Then from equation (3.24), one has

$$v_{jN}{}^{*}(t) = V_D F_j{}^{*}(t) \quad , j \in \{A,B,C\} \tag{3.25}$$

Thus, by taking the average over one switching period T_S as follows:

$$\frac{1}{T_S}\int_{t}^{t+T_S} v_{jN}{}^{*}(\lambda)d\lambda = \frac{V_D}{T_S}\int_{t}^{t+T_S} F_j{}^{*}(\lambda)d\lambda \tag{3.26}$$

one can get the corresponding steady state relation:

$$V_{jN}(t) = V_D D_j(t) \quad , j \in \{A,B,C\} \tag{3.27}$$

where

$$V_{jN}(t) \overset{\Delta}{=} \frac{1}{T_S}\int_{t}^{t+T_S} v_{jN}{}^{*}(\lambda)d\lambda \tag{3.28}$$

$$D_j(t) \overset{\Delta}{=} \frac{1}{T_S}\int_{t}^{t+T_S} F_j{}^{*}(\lambda)d\lambda \tag{3.29}$$

From the above results, it is seen that the inverter output voltage or current is sinusoidal, however, due to its low frequency variation as compared with the high switching frequency f_S, for each time instant, say t_k, one can use the equivalent duty ratio, $D_j(t_k)$ to achieve the input-output relation of equation (3.27) just like for a DC-to-DC converter. Similarly, assume that V_{jn} and I_j, $j \in \{A,B,C\}$ are the corresponding average variables as defined in equation (3.28), respectively. It follows that the resulting steady state model can be represented as shown in Fig. 3.6.

From Fig. 3.6, it is obvious that given the command signals, D_A, D_B, and D_C, one can obtain the resulting steady state output V_{jn} and I_j, $j \in \{A,B,C\}$ easily. However, for completeness, the block diagram inside the dotted frame is also given to show how to obtain the duty ratios of the virtual switches from the actual switching functions and current directions.

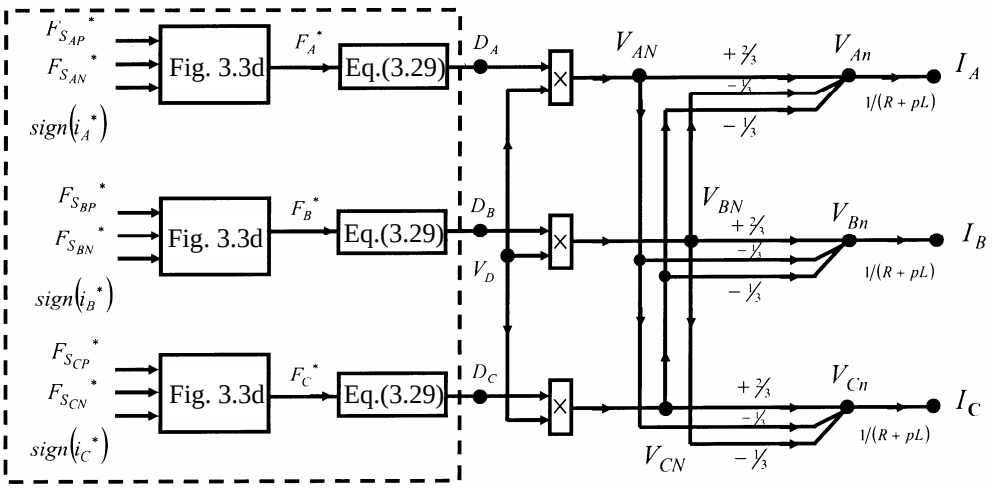


Fig. 3.6 The steady state model.

C. Small-signal Model

With the same assumption of assuming the inverter voltage frequency is much less than the switching frequency, one can use the same state space average technique to find the corresponding small-signal model in a similar way used for DC-to-DC converters. Let $\hat{d}_j$, $\hat{v}_D$, $\hat{v}_{jN}$, $\hat{v}_{jn}$, and $\hat{i}_j$, $j \in \{A,B,C\}$ represent the small

signals of the corresponding node variables of d_j, v_D, v_{jN}, v_{jn} and i_j, respectively. Then from equation (3.27), one has the following perturbed equation

$$\begin{aligned}\left(\hat{v}_{jN}+V_{jN}\right)&=\left(\hat{v}_D+V_D\right)\left(\hat{d}_j+D_j\right)\\&=V_D D_j+\hat{v}_D D_j+\hat{d}_j V_D+\hat{v}_D\hat{d}_j\end{aligned} \tag{3.30}$$

Therefore, from equation (3.30) one can obtain

$$\hat{v}_{jN}=\hat{v}_D D_j+\hat{d}_j V_D+\hat{v}_D\hat{d}_j \tag{3.31}$$

It follows that one can obtain the desired small-signal model as shown in Fig. 3.7. It should be pointed out here that to achieve better accuracy the nonlinear term in equation (3.31) is also included in Fig. 3.7. Naturally, the nonlinear term can also be neglected to get the familiar linear model.

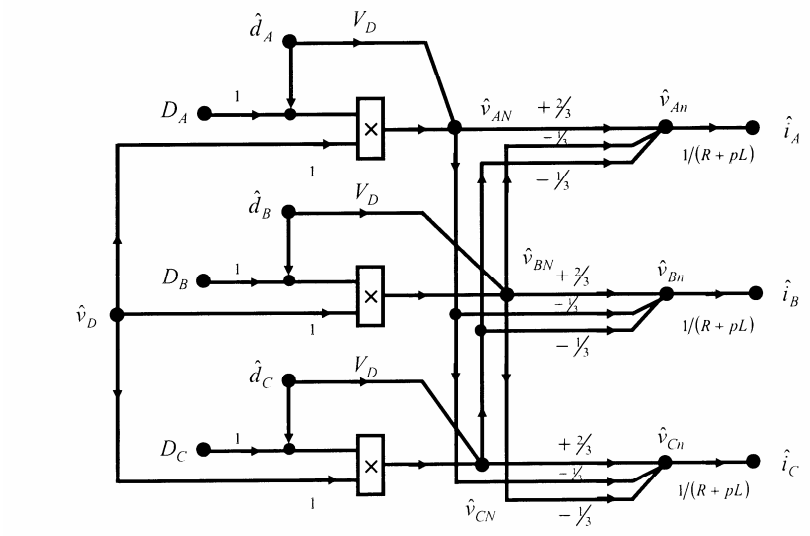


Fig. 3.7 The small-signal model.

3.4 Simulation Results

From previous results one can see that the structure of the resulting switching flow-graph model is very similar to the simulation structure of MATLAB/SIMULINK. Hence, it is quite easy to implement the model in MATLAB/SIMULINK environment to get the simulation results without requiring other extra efforts. As illustrations,

some examples are given below.

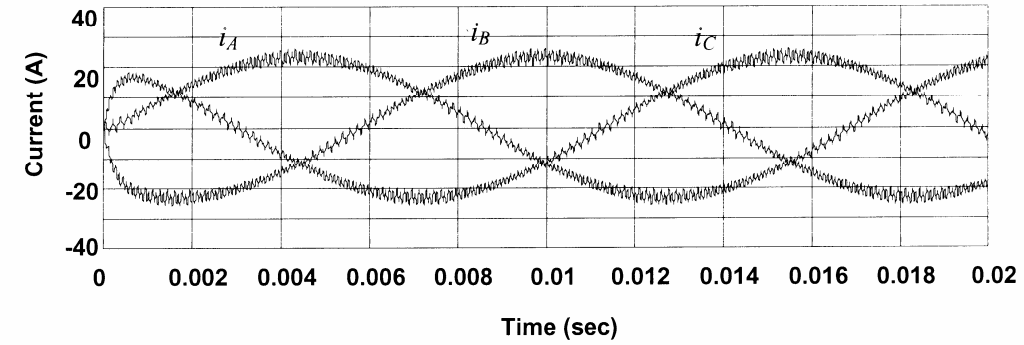
Example A:

First, consider the example with a Y-connected RL load as shown in Fig. 3.1, where $V_D = 500V$, $R = 6.2\Omega$ and $L = 0.15mH$. Assume the well known sinusoidal PWM is adopted with switching frequency $f_S = 6kHz$ and the amplitude of the triangular wave is $5V$. Also, the voltage command signals are given as follows:

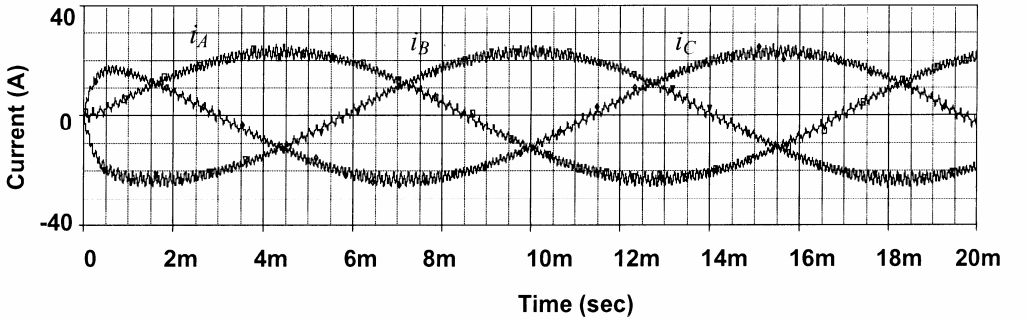
$$V^*_{an}(t) = 3\sin(120\pi t)$$
$$V^*_{bn}(t) = 3\sin(120\pi t - 120^\circ)$$
$$V^*_{cn}(t) = 3\sin(120\pi t + 120^\circ)$$

It follows that the corresponding switching functions of the six active switches, namely $F_{S_{jP}}$ and $F_{S_{jN}}$ can be obtained directly. Hence, by implementing Fig. 3.5 with MATLAB/SIMULINK using zero initial conditions, one can get the desired output currents as shown in Figs. 3.8(a) and 3.9(a) corresponding to zero and $20\mu s$ blanking time respectively. For comparison, the same example is carried out by using PSPICE and under the same conditions. The corresponding results are shown in Figs. 3.8(b) and 3.9(b) respectively. It is found that both simulation results agree with each other very closely. However, the computation time required by using the proposed switching flow-graph model is much less than that required by using PSPICE. For example, for the case with $20\mu s$ blanking time and with $100ms$ simulation time period, it takes only 7secs by using the proposed model as compared with 66secs by using PSPICE program when running a PC with Pentium IV 1.6G / 1500MB RAM and with $5\mu s$ step size.

Then, consider the dynamic performance simulation, the V_D is applied at t = $5ms$ and is decreased to 400 V at t = $35ms$. Also the RL load is changed to $R = 3.1\Omega$ and $L = 0.075mH$ at t = $65ms$. Figs. 3.10a and 3.10b show the output currents generated from the switching flow-graph model and the PSPICE model with zero blanking time respectively. Both simulation results agree with each other rather closely which reveals that the switching flow-graph model can correctly predict the dynamic response, such as the start up transient and load variation transient.



(a)



(b)

Fig. 3.8 Simulation results of the output currents with zero blanking time using (a) switching flow-graph model, (b) PSPICE model.

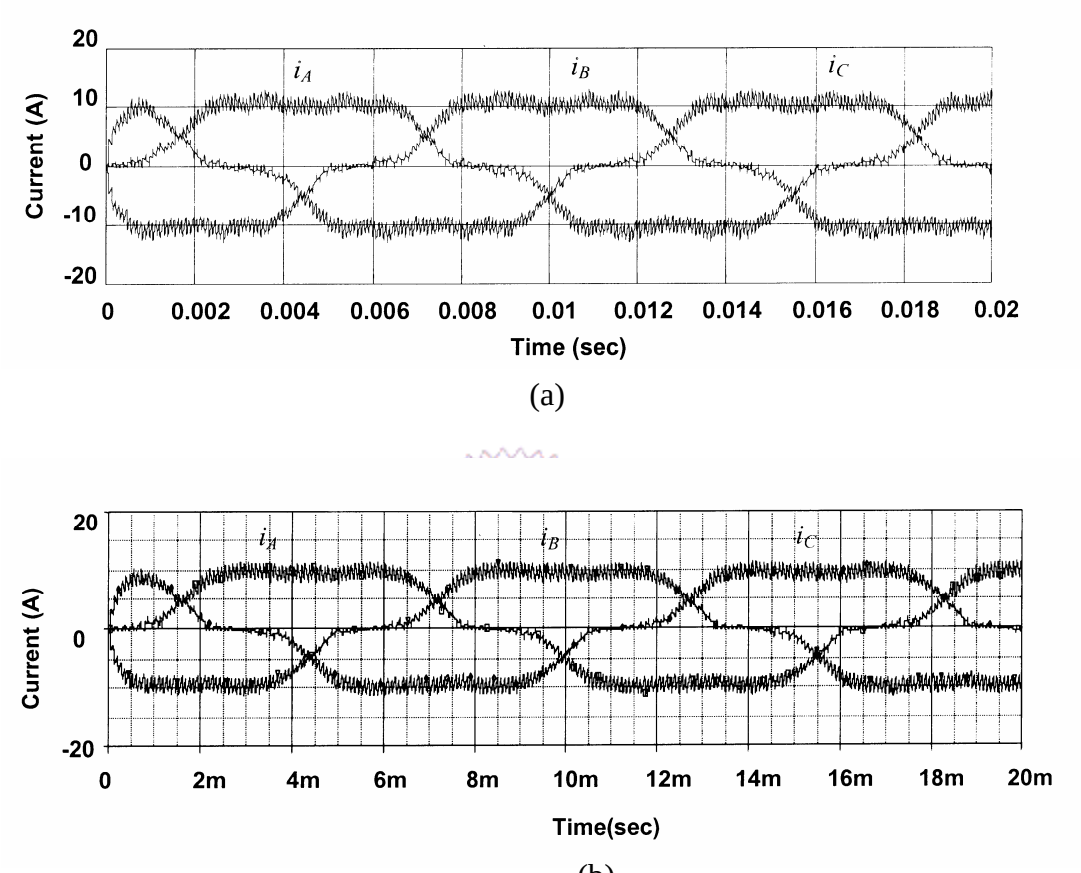
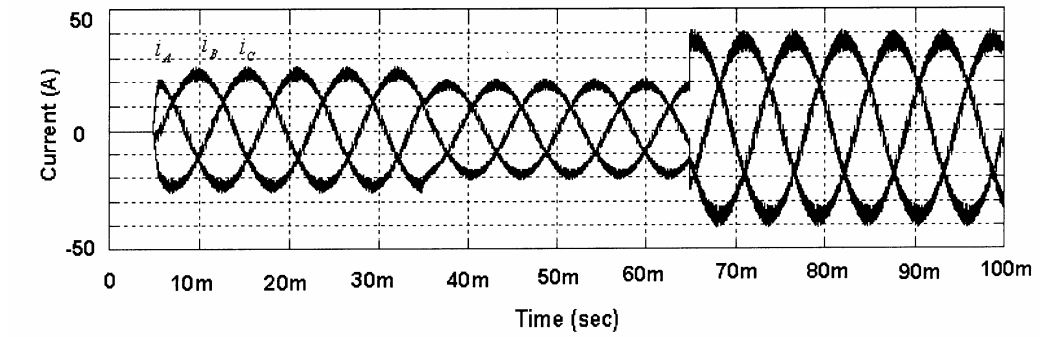
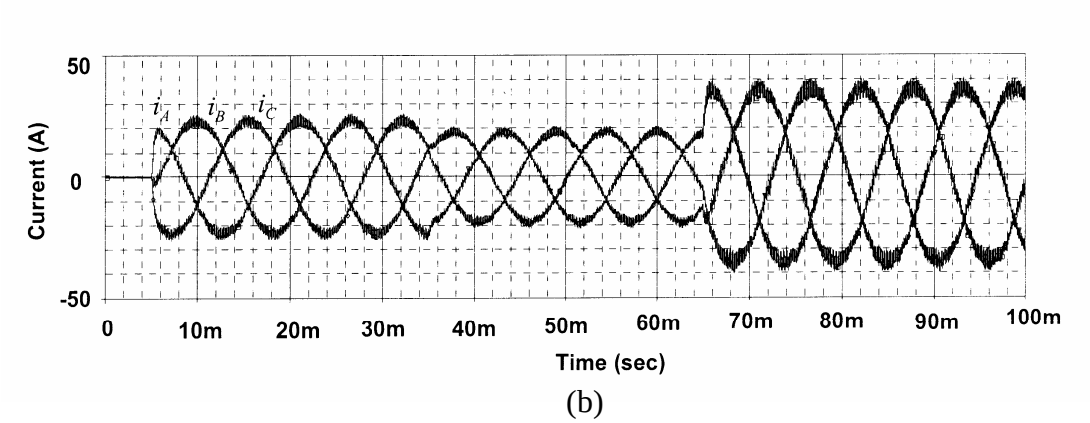


Fig. 3.9 Simulation results of the output currents with *20μs* blanking time using (a) switching flow-graph model, (b) PSPICE model.



(a)



(b)

Fig. 3.10 Dynamic simulation results of the output currents using (a) switching flow-graph model, (b) PSPICE model.

Example B:

Next, consider the second example to illustrate an application of the proposed switching flow-graph model to consider the ON-resistance of the active switches. Since an extra resistive voltage drop is generated for each active switch whenever a current is passed through that active switch, it is quite straightforward to add another virtual switching function F_{jR}, $j \in \{A,B,C\}$ to each arm to take care of this resistive voltage drop:

$$F_{jR}(t) = F_{S_{jP}} \quad OR \quad F_{S_{jN}}$$
$$j \in \{A,B,C\}$$

The resulting large-signal switching flow-graph is shown in Fig. 3.11 for reference.

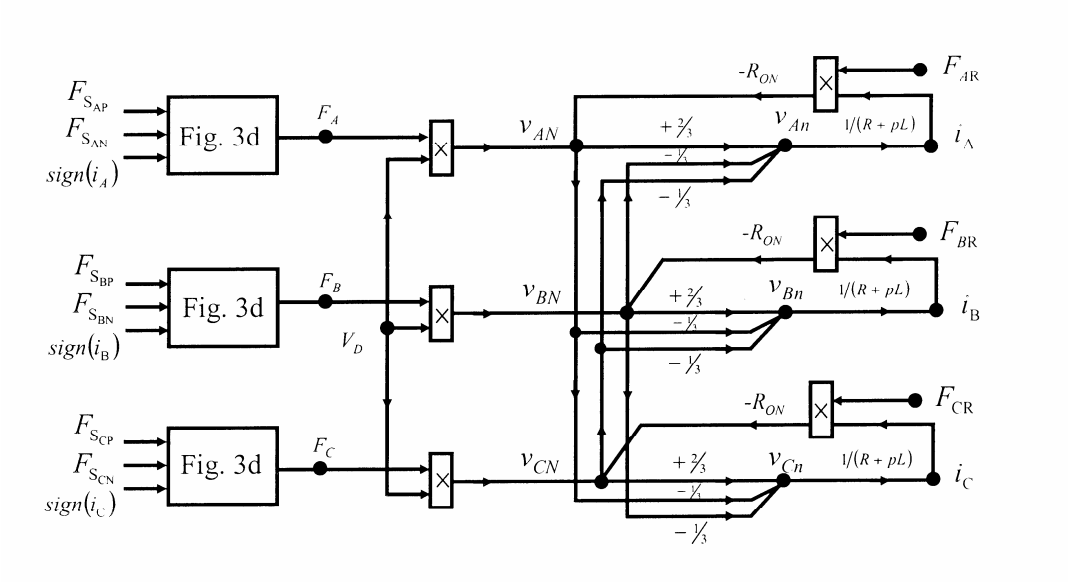
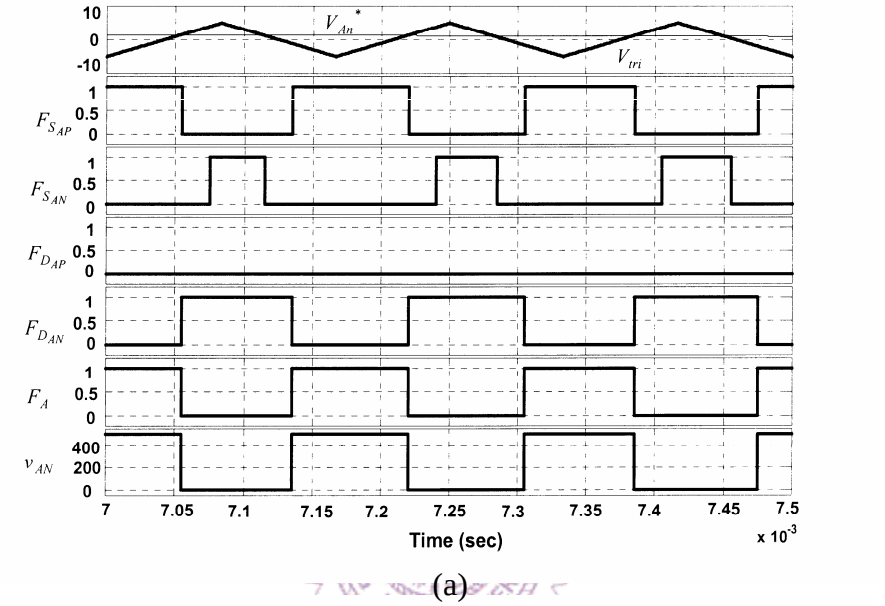


Fig. 3.11 The large-signal switching flow-graph model considering ON-resistance of active switches.

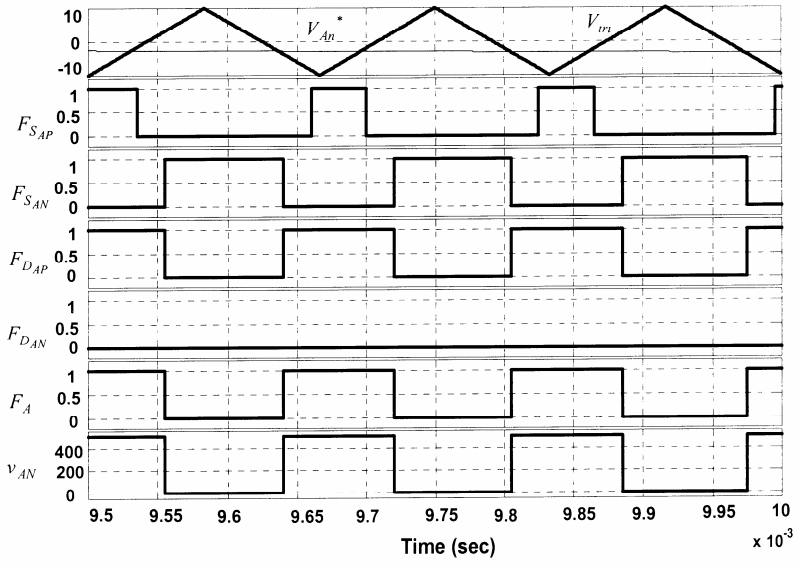
By using the same simulation conditions except including the ON-resistance of 0.23Ω for each active switch (according to the SPICE model of IRFP460 from PSPICE library), one can obtain the output currents. Due to the small value of ON-resistance, the output currents are basically similar to that of the previous example and will not be repeated here.

For reference, Fig. 3.12 also shows the waveforms of $F_{S_{AP}}$, $F_{S_{AN}}$, $F_{D_{AP}}$,

$F_{D_{AN}}$, F_{A} and v_{AN} for $i_A > 0$ and $i_A < 0$ for the case of $20\mu s$ blanking time. From $F_{S_{AP}}$ and $F_{S_{AN}}$ of Fig. 3.12, one can see that $F_{D_{AP}} = 0$ for $i_A > 0$ and $F_{D_{AP}} = \overline{F_{S_{AN}}}$ for $i_A < 0$ which indeed agree with equation (3.5) exactly. Finally, from F_A of Fig. 3.12, one can see that virtual switching function $F_A = F_{S_{AP}}$ for $i_A > 0$ and $F_A = F_{D_{AP}}$ for $i_A < 0$. Again, this result indeed agrees with equation (3.10) exactly.



(a)



(b)

Fig. 3.12 Waveforms of $F_{S_{AP}}$, $F_{S_{AN}}$, $F_{D_{AP}}$, $F_{D_{AN}}$, F_{A} and v_{AN} for (a) $i_A > 0$ (b) $i_A < 0$.

Example C:

Consider an induction motor load as given in [43] with the following parameters:

stator resistance $R_S = 3.41\Omega$, stator inductance $L_S = 0.1868H$,

rotor resistance $R_r = 3.41\Omega$, mutual inductance $L_m = 0.1728H$,

number of poles $P = 4$, rotor inductance $L_r = 0.1868H$,

$\mathrm{V_D} = 135V$, $\mathrm{f_S} = 3kHz$,

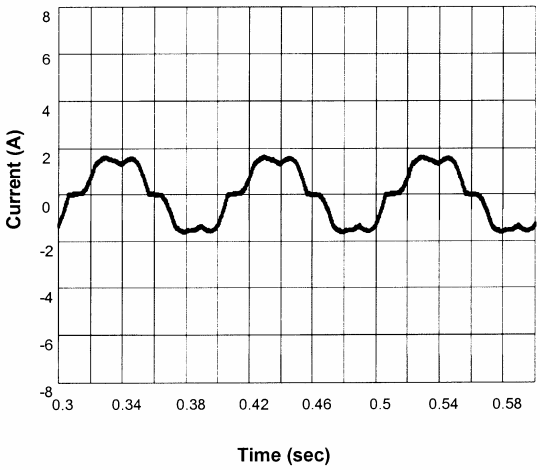
amplitude of triangular wave $= 15V$,

blanking time $= 40\mu\sec$.

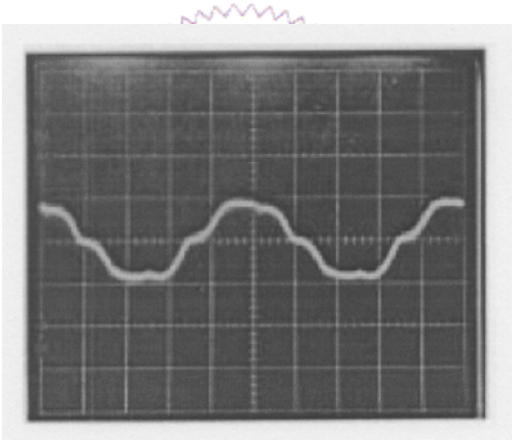
By using the proposed switching flow-graph model of Fig. 3.5 and implementing in MATLAB/SIMULINK environment with the above loading condition [43] and the following control signal

$$V^*_{an}(t) = 7.5\sin(20\pi t)$$
$$V^*_{bn}(t) = 7.5\sin(20\pi t - 120^\circ)$$
$$V^*_{cn}(t) = 7.5\sin(20\pi t + 120^\circ)$$

One can get the steady state output current waveform i_A as shown in Fig. 3.13(a). For comparison, Fig. 3.13(b) also shows the corresponding experimental result of [43]. From Figs. 3.13(a) and 3.13(b), one can observe that both results agree with each other closely. It is rather easy to simulate this inverter-fed motor system on the system-level evaluation.



(a)



(b)

Fig. 3.13 The steady state current waveforms of A-phase (a) simulation result (b) experimental result [43]. (horizontal 20ms/div, vertical 2A/div)