ABSTRACT

Significant advances in VLSI process technology have scaled the feature size down. As the transistor size shrinking, more and more transistors can be integrated into a single chip. To make large number of components in a chip working together, processor-based design methods have become one of the best choices. In a processor design, power consumption and performance are two important issues. The power and performance issues are related to the execution of an instruction. During the execution of an instruction, three main steps are fetching, decoding, and executing. We will propose techniques to improve performance and power in these three steps.

First, for the step of fetching instructions, because the advances of technology shorten the distances between wires, the crosstalk problem has affected the wire delay seriously. Since the data sequences on an instruction bus are known during the compile time, we present two compiler algorithms, rescheduling and renaming, for performance improvement by eliminating crosstalk effects on an instruction bus.

Second, for the step of decoding instructions, we found that the execution frequency of instructions is uneven. It means that in most of time, we need not utilize the whole instruction decoder to decode instructions. By tracing program execution sequences, we decompose the instruction decoder into several coupling sub-decoders. For most of time, only one sub-decoder is activated and the power is minimized.

Finally, for the step of executing instructions, the multiplication is the most power consuming operation among all operations in an instruction set. Based on a dual-&-configurable-multiplier structure, our proposed method devises a multiplication instruction-set for low-power ASIPs. Our method exploits the execution sequences of multiplication instructions and effective bit-widths of variables to reduce power consumed by redundant multiplication bits.