中文摘要

電力的消耗長期以來一直是現代積體電路設計的重要考量。這篇論文中，我們提出對於時脈樹之電力優化技巧，使用多位元正反器及降低總線路長度這兩者來達成目標。我們經由合併多個單位元正反器成為多位元觸發器，有效降低正反器的電力消耗；除此之外，透過謹慎的選擇正反器合併組合與合併後的擺放位置，總線路長度在合併後也能大幅降低。兩者合併的效用能有效大幅減少時脈樹的電力消耗。

Abstract

Power optimization has always been an important issue for modern IC design. In this paper, we present a power optimization technique for clock tree by applying multi-bit flip-flops and reducing total wire length. Through merging flip-flops into MBFFs, we effectively reduce power consumption caused by clock buffers. Moreover, by judiciously merging and placing the MBFFs, the total wire length is also significantly reduced. The combined effect of both techniques leads to a strong reduction in total power consumption of the clock network.