Chapter 6

Experiments

6.1 Experiment Setup

15 benchmark examples are selected from SPEC2000 suites [6]. The benchmark examples are first simulated with *SimpleScalar* [11] which simulates a super-scalar processor with out-of-order issue and execution. Alpha 21364 is chosen as the base processor for temperature analysis. Next, *Wattch* version 1.02 [5] is used as an analysis tool for architectural level power modeling and *HotSpot* [4] version 3.0 as a thermal analysis tool for temperature computation. Fig. 6.1 illustrates our experimental flow. Initial die temperature is assumed to be 60°C. 200 by 200 grid size is chosen for *HotSpot* temperature analysis and the subsequent sensor placement. Area of Alpha 21364 processor is $3cm^2$ and area ratio of *BJT* to *CORE* is 1:80.

In this experiment, the weighting factors α and β in Eq. (5.7) are 0.8 and 0.2, respectively and the weighting factors in Eq. (5.6) are W_1=0.06, W_2=0.03, W_3=0.13, W_4=0.26 and W_5=0.52.

We apply ±20% variation in constant current source. In other words, the current to *BJT*'s varies from $8uA$ to $12uA$ ($10uA$ in average). Moreover, 3 process corners, SS (both PMOS and NMOS are in slow corner), TT (both in typical corner) and FF (both in fast corner) are applied for temperature measurements. In our simulations, both current variations and process corner variations occur.

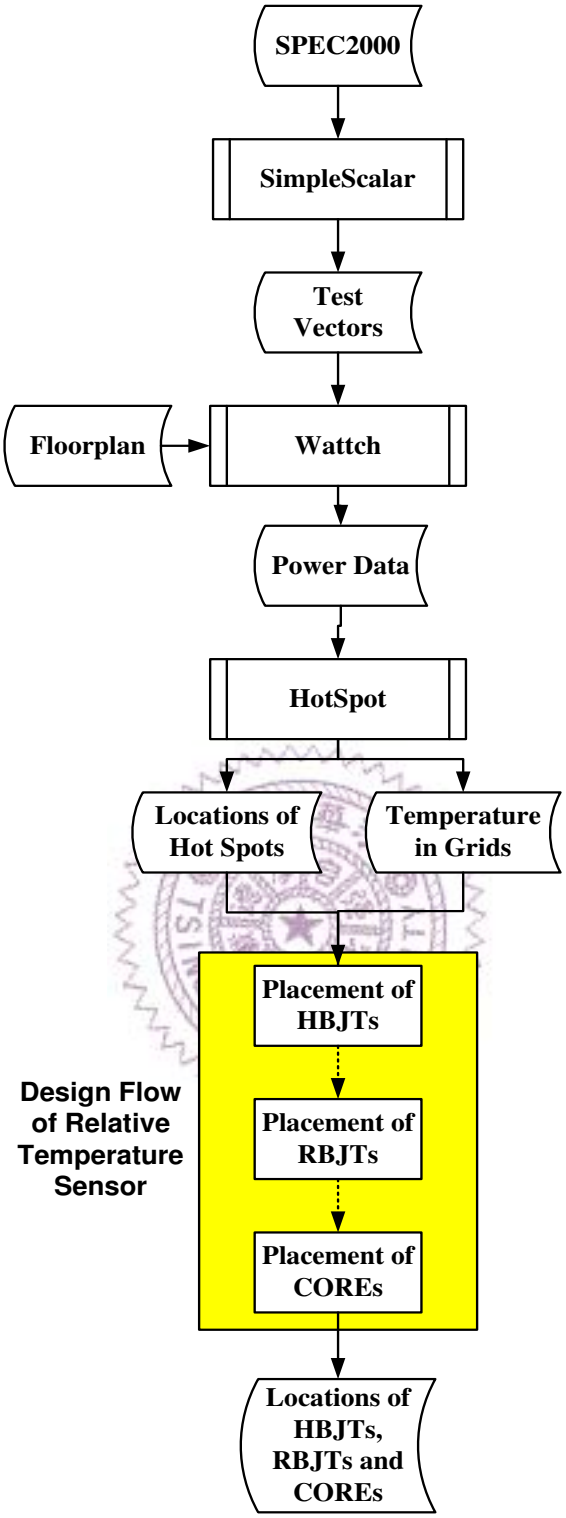

Figure 6.1: Simulation flow of placement to relative temperature sensors

Table 6.1: Comparison of Temperature Errors

	Min Error (°C)			Max Error (°C)		
Benchmark	ABS	REL	Ratio	ABS	REL	Ratio
wupwise	0.2010	0.0012	165	19.41	2.26	9
mgrid	0.2241	0.0013	176	19.51	2.33	8
applu	0.1794	0.0011	162	19.18	2.03	9
swim	0.1864	0.0011	165	19.23	2.07	9
galgel	0.1770	0.0011	157	19.16	2.01	10
facerec	0.2067	0.0012	167	19.45	2.30	8
lucas	0.2313	0.0013	182	19.50	2.33	8
vpr	0.0637	0.0007	91	18.34	1.29	14
eon	0.2447	0.0013	193	19.24	2.07	9
vortex	0.2623	0.0015	174	19.81	2.64	8
sixtrack	0.1835	0.0011	164	19.21	2.06	9
gap	0.0109	0.0000	271	17.97	0.95	19
gcc	0.1433	0.0023	61	21.00	3.67	6
fma3d	0.1642	0.0023	72	21.43	4.06	5
twolf	0.0024	0.0003	8	17.57	0.58	30
Average	-	-	147	-	-	11

6.2 Experiment Results

The first experiment is to compare the errors reported from *absolute* and *relative* temperature sensors. Table 6.1 shows the results. Maximum temperature errors and minimum temperature errors for each benchmark using placement of *absolute* temperature sensors by K-mean clustering [1] and placement of *relative* temperature sensors by our proposed algorithm are presented. The first column shows the name of SPEC2000 benchmark. The second and third columns give the minimum errors for *absolute* temperature sensor and *relative* temperature sensor, respectively, under assumed process variations. The fifth and sixth columns represent the maximum errors. The fourth and seventh columns show the ratio of temperature accuracy in minimum error and maximum error, respectively. The columns labeled *Ratio* is computed by $\frac{Error\,of\,ABS}{Error\,of\,REL}$. From the table, we can see that *relative* temperature sensor outperforms *absolute* temperature sensor in temperature accuracy. *Relative* temperature sensor shows 147 times improvement in minimum error cases and 11 times improvement in maximum error cases.

Table 6.2: Summary of area reduction and interconnection overhead

	ABS	REL	Ratio
Area of Sensors (unit of BJTs)	1620	425	0.26
Length of Interconnection (mm)	0	7.42	-

The next experiment is to understand area reduction and interconnection overhead by using *relative* temperature sensor. The results are summarized in Table 6.2. The second row shows the area reduction of *relative* temperature sensor from 1620 units to 425 units, where unit is the area of one *BJT*. The column labeled *Ratio* is computed by $\frac{Area\,of\,REL}{Area\,of\,ABS}$. It can be seen that 74% reduction in area is achieved. The third row is the interconnection overhead caused by *relative* temperature sensor. Assuming chip area is $3cm^2$, the interconnection overhead of metal length is about $7.4mm$.