# Chapter 1

# Introduction

Reducing power dissipation is one of the most important issues in VLSI design today. The average dynamic power consumption is given by Equation (1.1),

$$P_{avg} = \frac{1}{2} V_{dd}^2 f \Sigma_v C(v) \cdot E(v) \tag{1.1}$$

where $C(v)$ is the loading capacitance, $E(v)$ is the switching activity at the output of gate $v$, and $f$ is the clock frequency. By lowering the supply voltage ($V_{dd}$), dynamic power can be reduced quadratically from Equation (1.1). But, reducing $V_{dd}$ degrades circuit performance. In Equation (1.2), scaling down the threshold voltage ($V_{th}$) is one method to maintain circuit performance for lower power supply.

$$Delay = \frac{C_{load} V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \tag{1.2}$$

However, scaling down the $V_{th}$ will make the subthreshold leakage current increase exponentially [1]. This makes large static power consumption in cut-off region. In [2], sub-threshold leakage power accounts for 42% of total power in 90nm technology. Therefore, reducing leakage power becomes more and more important.

Several researches are focused on reducing leakage power. One strategy is dual threshold voltage (dual-$V_{th}$) design. It uses low $V_{th}$ transistors for gates on the critical path and high $V_{th}$ transistors on the non-critical path [9]. Using high $V_{th}$ gates on the non-critical path will significantly reduce leakage power consumption without violating the timing constraint.

Another strategy is Multi-Threshold CMOS (MTCMOS) design [1, 11, 12, 13]. The MTCMOS circuit structure is illustrated in Figure 1.1. Low $V_{th}$ modules are connected in series with a high $V_{th}$ transistor called "sleep transistor", and the line connected between low $V_{th}$ modules and a high $V_{th}$ transistor is called "virtual ground". The *SLEEP* signal is used to control the sleep transistor in active or standby mode. In active mode ($SLEEP = 0$), the sleep transistor is turned on to retain functionalities and low $V_{th}$ module maintains circuit performance at low power supply. In sleep mode ($SLEEP = 1$), the sleep transistor is turned off and this reduces leakage current because the leakage current only from high $V_{th}$ sleep transistor which

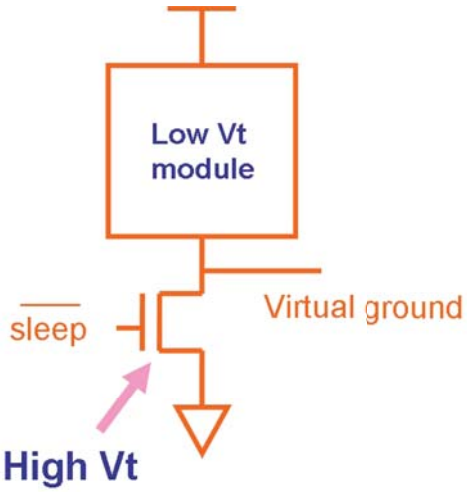


Figure 1.1: MTCMOS circuit structure

is very low. Proper sleep transistor sizing is an important factor affecting the area, power consumption and performance of the circuit [1].

In this thesis, we focus on the standard cell placement with MTCMOS circuit. We propose two standard cell placement algorithms to minimize total wirelength overhead and sleep transistor size. The first one is a functionality directed placement algorithm and the second one is a direct placement with iterative cell moving algorithm.

The rest of the thesis is organized as follows. Chapter 2 will present the related work and our motivation. Our method will be shown in Chapter 3. Benchmark results are shown in Chapter 4. Finally, conclusion remarks are drawn in Chapter 5.