Chapter 2

Related Work on MTCMOS and Our Motivation

In this chapter, we first introduce some concepts on sleep transistors in Section 2.1. Then, related work on MTCMOS and our motivation are described in Section 2.2.

2.1 Use of Sleep Transistors

During the active mode, the sleep transistor can be modeled as a resistor R as shown in Figure 2.1 [12]. This generates a small voltage drop V_x equal to IR where I is the current flowing through the sleep transistor. Voltage drop reduces the driving capability of gate from V_{dd} to $V_{dd} - V_x$, and this degrades the performance of the circuit. If the discharge current I is large, the resistor R should be made small to maintain performance, and consequently, the size of the sleep transistor be made large. This causes the expense of

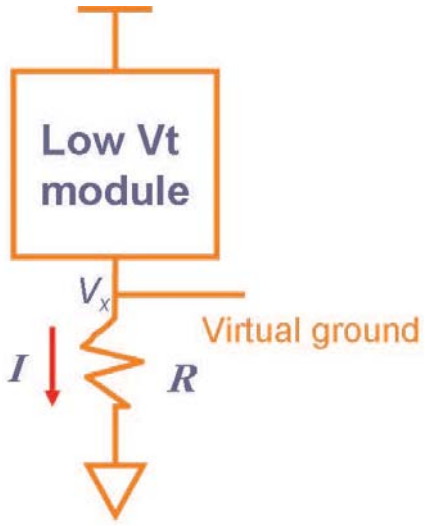

Figure 2.1: Sleep transistor modeled as resistor

extra area and power. On the other hand, if the sleep transistor is sized too small, the performance of circuit degrades. Therefore, the sleep transistor sizing problem is important in the MTCMOS design. Moreover, the current I flowing through the sleep transistor is the main factor to determine the size of sleep transistor to maintain required performance. The worst case scenario takes place if all cells supported by the sleep transistor discharge current simultaneously (Figure 2.2). The sleep transistor is thus sized up to sustain the sum of the discharge current ($I = I1 + I2 + I3$). However, if these cells are mutual exclusive discharge, the sleep transistor is sized according to the maximum current of these cells ($I = max\{I1, I2, I3\}$). In this case, the

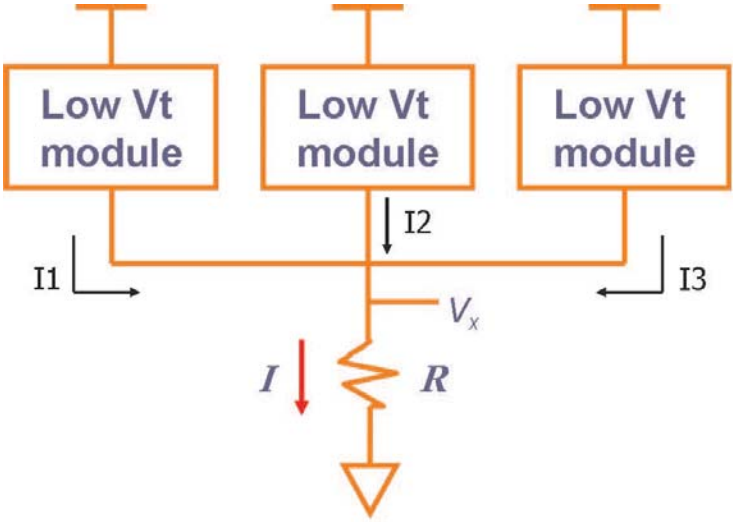

Figure 2.2: Discharge scenario

size of sleep transistor is much smaller.

2.2 Related Work on MTCMOS and Our Motivation

A single and large sleep transistor to accommodate the whole circuit was proposed in [11]. Sharing a single sleep transistor for the whole circuit causes long virtual ground wires for distant cells. Therefore, the sleep transistor should be sized larger than expected to compensate for the added resistance of virtual ground wires.

In addition, distributed sleep transistors were proposed in [1, 13]. The efforts were to cluster cells so that mutual exclusive discharge cells are clus-

tered together to share one sleep transistor. This distributed sleep transistors can avoid long virtual ground wires. The sleep transistor is sized according to the maximum current of clustered cells.

One disadvantage of these cluster-based approaches is that the size of sleep transistors are overestimated because only the circuit topology is considered. An example in [3] shows that even if two cells may make transitions at the same time, two cells may not discharge at the same time owing to the consideration of circuit functionality. Therefore, a *functionality directed clustering technique* is proposed in [3]. This method takes both topology and functionality into consideration. The result shows that this method can achieve on the average 18% reduction ratio in terms of the size of sleep transistors as compared the method without considering functionality.

From [3], we know that clustering cells to share sleep transistors taking both topology and functionality into consideration can effectively reduce the number of sleep transistors. However, this clustering technique do not consider the placement issue. Two cells not in the same cluster in the MTCMOS design may be timing critical or strongly connected. This will cause the increase of the total wirelength. The wirelength overhead may result in the violation of timing constraint, more power consumption...etc. For this reason, the placement issue should also be considered in the cluster-based MTCMOS

design. Therefore, we propose a cell placement algorithm for cluster-based MTCMOS design to simultaneously minimize wirelength overhead and sleep transistor size.