Chapter 1

Introduction

Power consumption has become one of the most important design considerations in circuit design recently. In general, power sources are classified as dynamic and leakage power. Studies on low power design are abundant in the literature [3, 4, 5, 6] in which various techniques have been proposed to minimize either dynamic power or leakage power.

One design problem is modelled as "Under a timing constraint, minimize the power as much as possible". To solve this problem, one direction of research is focused on minimizing the dynamic power. The minimization is based on the dynamic power consumption model, which is shown in Equation (1.1).

$$P_{avg} = \frac{1}{2} \cdot C \cdot V_{dd}^2 \frac{\cdot E}{T_{cycle}} \tag{1.1}$$

where C is load capacitance, V_{dd} the supply voltage, T_{cycle} the clock period, and E the transition density. In these approaches, to maintain the perfor-

mance, sizes of gates on critical paths usually remain unchanged while gates on non-critical paths are sized down to utilize their timing slack. By doing so, the gate capacitance is reduced so is the dynamic power consumption.

The other direction is focused on reducing leakage power consumption by dual threshold assignment. It uses low-Vth transistors for gates on the critical-path and high-Vth transistors on the non-critical-path. This strategy is used in [3, 4, 5, 6] and has shown that it has significant saving of leakage power and dose not mitigate the performance of the circuits.

Simultaneously gate sizing and threshold assignment has been studied in [8] for low power design. However, this research focuses on slack assignment on non-critical path.

Gate sizing will increase more gate capacitance and hence large dynamic power and minor leakage. On the other hand, re-assigning Vth will cause large leakage power increase. However, given a timing constraint, to minimize total power consumption including active mode (dynamic and leakage power) and idle mode (leakage power), optimization algorithm must be able to utilize sizing and threshold voltage assignment two techniques interchangeable to obtain the best gain.

We find that switching activity of a gate plays an important role in making decision as to choosing gate sizing or threshold assignment. For high switch-

ing density gates, re-assigning Vth should be used while for low switching density gates, gate sizing should be utilized. By considering both techniques at the same time taking switching activity into account, we can minimize the total power of the circuit both on critical path and non-critical path.

The rest of the paper is organized as follows. Chapter 2 will present related work and our motivation. Algorithm taking switching activity into consideration for sizing and threshold voltage assignment will be shown in Chapter 3. Benchmark results are presented in Chapter 4. Finally, conclusion remarks are drawn in Chapter 5.