Chapter 5

Conclusions

We have studied the problem that under a timing constraint, to minimize total power consumption including dynamic and leakage power (active mode) and leakage power (idle mode). Our optimization algorithm is able to utilize sizing and threshold voltage assignment two techniques interchangeable to obtain the best gain. We have found that switching activity of a gate plays an important role in making decision as to choosing gate sizing or threshold assignment to improve timing performance. For high switching density gates, Vth assignment should be used while for low switching density gates, gate sizing should be utilized. We have developed an algorithm to perform gate sizing and threshold voltage assignment simultaneously taking switching activity into consideration. The results have shown that under the timing constraint, our method can achieved 16.26%, 18.53%, and 26.70% improvement as compared the original circuits for cases the fraction of active time

are 100%, 50%, and 10%, respectively.