Chapter 2

Related Work and Our Motivation

In this chapter, we will review some power reduction techniques and introduce our motivation.

2.1 Related Work

As we know, a transistor with low threshold voltage has more leakage power and fewer delay than that with high threshold voltage. A simple way to take advantage of this property is to use low Vth cell on critical path and high Vth cell on non-critical path. This strategy is used in [3, 4, 5, 6] and has shown to gain significant saving of leakage power and dose not affect the performance of circuit. However, Vth assignment researches only consider about saving leakage power consumption instead of total power consumption.

Meanwhile, gate downsizing cells on non-critical path is also a powerful

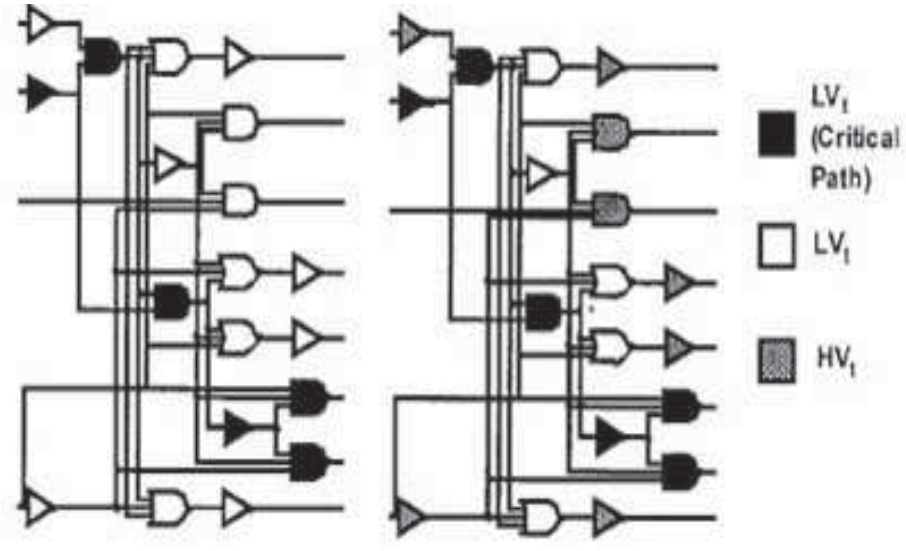


Figure 2.1: Reassign Vth of gates which are on non-critical paths.

technique to minimize power. In [8] simultaneously assigning threshold voltage and size of gate was proposed to minimize total power savings. The basic idea of its algorithm is to make full use of slacks cells on non-critical path to resize or re-assign Vth of gate.

Most of previous work models power consumption issue as a slack assignment problem. Main focus was on how to use slacks in circuit to achieve the greatest power saving. In other words, only gates on non-critical path can be re-synthesized to save power consumption.

2.2 Our Motivation

To enhance the performance of a circuit, we can size-up cells or change the Vth of cells from high to low. The former method will increase dynamic power and small leakage power while the latter method increases leakage power.

We observe that achieving the same timing performance and lower power, whether to use up-sizing or lower Vth techniques is determined by the switching activity of a gate. If a cell has high switching activity, lowering Vth techniques should be used while for low switching activity cell, up-sizing is a better selection.

To understand if our observation is correct, we perform an experiment on two invertors. The first inverter A has higher Vth than inverter B. But the size of B is smaller than that of A. The size and Vth are turned so that they have the same delay under the same output loading. The experiment is performed using the *45nm* model provided by *PTM*[9] and simulated by *Hspice*. The result is shown in Figure 2.2. In this figure, Y axis is the power reduction ratio, $\frac{B-A}{B}$ and X axis is the switching activity of the invertors. The figure shows that when the switching activity is lower than 20%, using inverter A (high Vth and larger cell) will produce less amount of total power. However, when the switching activity is more than 20%, inverter B (low Vth

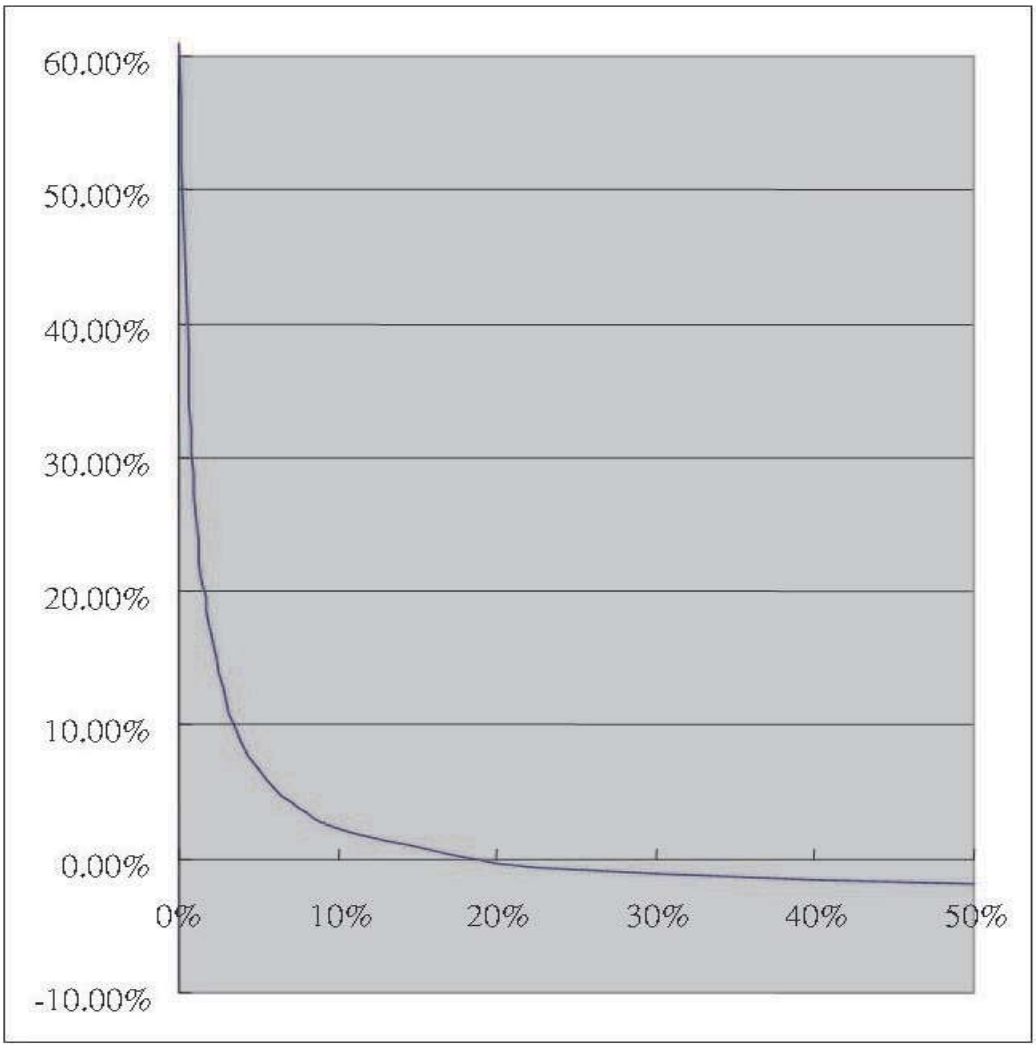
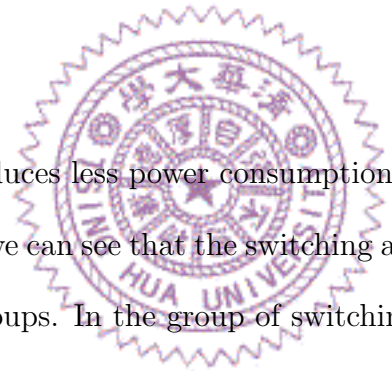


Figure 2.2: Relation between switching activity and power reduction rate.

Table 2.1: Switching activity distribution of cells

Switching activity(α)	Ratio(%)						
	TOP	MAC	AVG	GCC	RSA	AES	Average
$0\% \leq \alpha \leq 20\%$	74.90	55.02	67.08	52.97	71.39	56.83	63.03
$20\% \leq \alpha$	25.10	44.98	32.92	47.03	28.61	43.17	36.97



and smaller cell) produces less power consumption.

From Figure 2.2, we can see that the switching activity of gates are indeed distributed in two groups. In the group of switching activity less than 20%, a cell with high Vth and larger gate size is power efficient while in the group of switching activity more than 20%, a cell with low Vth and smaller size is better.

Next, we would like to know how the switching activity distributes for all cells. Table 2.1 shows switching activity distribution of cells in a set of circuits. In average, 63.03% cells are with switching activity between 0% to 20%.

Moreover, previous work focused on minimizing power on non-critical path. But, we can minimize power both on critical path and non-critical path. On critical path, we can re-assign Vth to high and up-size gates which has small switching activity. On non-critical path, slack can be used to down-size gate or assign Vth to high.