

Contents

1	Introduction	3
2	Related Work and Our Motivation	6
2.1	Related Work	6
2.2	Our Motivation	8
3	Gate Sizing and Threshold Voltage Assignment	12
3.1	Problem Definition and Design Flow	12
3.2	Algorithm for Gate Sizing and Threshold Voltage Assignment	15
3.2.1	Critical Path	15
3.2.2	Non-Critical Path	23
4	Experimental Results	28
5	Conclusions	35