Abstract

Power consumption has become one of the most important design considerations in circuit design recently. One design problem is modelled as "Under a timing constraint, minimize power as much as possible". Previous research focused on either minimizing the dynamic power by down sizing nodes on non-critical paths to utilize their timing slack, or reducing leakage power consumption by dual threshold assignment by using high-Vth gates on the non-critical path. However, given a timing constraint, to minimize total power consumption including active mode (dynamic and leakage power) and idle mode (leakage power), optimization algorithm must be able to utilize sizing and threshold voltage assignment two techniques interchangeable to obtain the best gain. We find that switching activity of a gate plays an important role in making decision as to choosing gate sizing or threshold assignment. For high switching density gates, Vth assignment should be used while for low switching density gates, gate sizing should be utilized. We develop an algorithm to perform gate sizing and Vth assignment simulta-

neously taking switching activity into consideration. The results show that under the same timing constraint, our method can achieve 16.26%, 18.53%, and 26.70% improvement as compared the original circuits while the fraction of active time are 100%, 50%, and 10%.