Chapter 5

Conclusions

Based on Starfish, we proposed a set of new instructions and architecture to improve the performance of interpolation. We implement the data path in Verilog and verify the functionality. The synthesis result shows that the timing constraint is met with area-overhead of 12.84% in DAG stage and 143.21% in DA stage. New instructions are added to Starfish tool-chain and applied to interpolation procedure. Experimental result shows that we can improve the performance improvement up to 45% on interpolation procedure with our new instructions.