摘要

隨半導體技術之演進，訊號線延遲已支配整體電路延遲並成為電路效能之瓶頸。為提升效能，半導體業已投入大量心力於晶片微型化技術，藉以縮短訊號線長度。在本論文中，我們提出利用先進微影技術與三維晶片整合技術將晶片尺寸縮小。由於相位移光罩技術為一有效之先進微影技術，我們將著重於相位移技術並提出以訊號線擴展方式修正光罩以利佈局合乎相位移光罩設計規範。實驗結果顯示，我們的演算法可以消除 98%的相位衝突而不需增加晶片面積。

由於直通矽穿孔技術之發展，使得三維整合技術得以縮短介晶片連線之長度並提高晶片效能。然而直通矽穿孔占據可觀之晶片面積並且需要規劃擺放位置。若於早期實體設計時未先規劃直通矽穿孔之位置，則須依靠後置處理之方式將直通矽穿孔分配於晶片上未使用之區域內。因此，我們提出一同時擺放模組區塊與直通矽穿孔之三維平面規劃演算法。實驗結果顯示，相較於一後置處理配置直通矽穿孔之平面規劃演算法，我們提出之三維平面規劃演算法可縮短 22.3%之訊號線長度。

雖然直通矽穿孔可有效減低三維晶片之連線長度，但其所占據之面積亦對線路產生負面衝擊。使用過多直通矽穿孔將增加三維晶片之面積，並延長訊號線長度。因此，我們提出一評估方法研究三維晶片中訊號線長與直通矽穿孔數量與尺寸之利弊分析。當直通矽穿孔之尺寸較小，使用較多之直通矽穿孔有利於訊號線長度之縮減。反之，當使用較大之直通矽穿孔，則適合使用最少數量之直通矽穿孔繞線已減小總體訊號線長度。此外，我們的實驗亦顯示最佳之三維晶片分割策略也隨直通矽穿孔之尺寸改變。當使用越大的直通矽穿孔，則必須越早分配邏輯閘於不同層中。

Abstract

As the semiconductor technology advances, the interconnect delay gradually dominates the entire circuit delay and becomes the bottleneck of the circuit performance. To further improve the performance, manufacturers invest great deal of effort to reduce the delay by miniaturizing the chip size and shortening the interconnects. In this dissertation, we propose using modern lithography and 3D integration technologies to scaling down the chip size. Since the phase shift mask(PSM) is a very effective lithography technology to miniature the layout patterns, we focus on PSM design issues and propose a wire spreading algorithms to modify layouts for PSM compliance. Experimental result shows that our algorithm can eliminate more than 98% of phase conflicts without increasing the die size.

With the aid of through-silicon via (TSV), 3D integration is able to shorten the wirelength of inter-tier net and achieves high performance. However, TSV is not volumeless point and cannot be placed anywhere on a layout. Without planning TSVs in the early design stage, a post TSV insertion procedure is required to arrange TSV to white space. To this end, we also propose a 3D floorplanning algorithm to simultaneously plan functional blocks and TSVs. Experimental results show that our algorithm outperforms a post-processing TSV planning algorithm in wirelength by 22.3%.

Although TSV potentially reduces the wirelength of a 3D-IC, the area overhead of TSV poses negative impact to circuit. Applying too many TSVs in a design increases the size of a 3D-IC and extends the distances among active devices. Therefore, we also propose evaluation methods to study the trade-off among wirelength, number of TSVs, size of TSVs and placement of 3D-ICs. Experimental results reveal that the optimal number of TSVs of a design varies with the size of TSVs. When the size of TSV is small, the using more TSVs is beneficial for wirelength reduction. On the contrary, when large TSV is applied, a design prefers using routing topologies with least number of TSVs to minimize the total wirelength. Also, our experimental results show that the best partition scheme for placement is sensitive to the size of TSV. The larger TSV we use, the earlier we have to partition cells to different tiers.