Chapter 5

Conclusions

We have presented a design flow for sizing sleep transistors in MTCMOS circuits under a specified performance degradation. Gates are clustered to share one sleep transistor. The relations of gates are modeled as a *relation graph* taking both topology and functionality into consideration. Clustering of gates is formulated as a clique partitioning problem. The results show that the proposed method can achieve on the average 20% and 18% reduction ratio in terms of the number of cliques and sleep transistors as compared the method without considering functionality.