Chapter 4

Experimental Results

Our algorithm, presented in Section 3, is implemented in the C language and executed on a SUN Sparc Workstation. Several MCNC and ISCAS benchmark circuits were tested to show the effectiveness of our algorithm. The experiment is performed using the gate type in *mcnc.genlib* of MCNC general library. SPICE simulation is performed for the gates using TSMC spice model of 0.18 μm technology. The maximum current of one sleep transistor is computed as 432uA under $(\frac{W}{L})_{sleep} \approx 10$ to have only 5% degradation in circuit performance. The input circuit is in gate level description. After cell characterization, our algorithm was performed to the circuit and produced an output of the clustered circuit.

Table 4.1 shows the statistics of our benchmark set. The column labeled **Gates** stands for the number of gates of circuits. The column labeled **In** and **Out** shows the numbers of inputs and outputs, respectively.

Table 4.1: Characteristics of benchmark

Circuits	Gates	In	Out
x2	66	10	7
9symml	246	9	1
apex7	268	49	37
i4	270	192	16
C432	287	36	7
xxx	287	36	7
example2	343	85	66
C880	424	60	26
alu2	433	10	6
i5	448	133	66
C499	542	36	7
C1355	590	41	32
C1908	724	33	25
rot	752	135	107
apex6	754	135	99
alu4	830	14	8
x3	1089	135	99
C3540	1426	50	22
C6288	2353	32	32
C5315	2437	178	123

To understand how effective of our proposed algorithm, we compare our design flow with functionality check to that with only topology check. Table 4.2 shows the results. The column labeled **T** are the result of design flow with only topology information. The column labeled **T+F** are the results taking both topology and functionality into consideration. The column labeled **# clique** is the number of cliques after the step of clique partitioning and the column labeled **# sleep trans** is the number of transistors after the step of merge of cliques. The column labeled **c_red** is the reduction ratio in terms of the number of cliques taking functionality into consideration and it is computed by:

$$c\_red = \frac{(\#clique_T - \#clique_{T+F})}{\#clique_T} \times 100\%$$

Similarly, the column labeled **s_red** is the reduction ratio in terms of the number of sleep transistors taking functionality into consideration and it is computed by:

$$s\_red = \frac{(\#sleep\ trans_T - \#sleep\ trans_{T+F})}{\#sleep\ trans_T} \times 100\%$$

The results show that the number of sleep transistors is over-constrained if only topology is considered. It results in more sleep transistors. Taking functionality into consideration, more gates can share one sleep transistor. The reduction in terms of the number of sleep transistors can be as high as

Table 4.2: Results of design flow with and without functionality information

Circuits	# clique			# sleep trans		
	T	T+F	c_red(%)	T	T+F	s_red(%)
x2	21	19	9	8	7	12
9symml	91	87	4	28	26	7
apex7	82	79	4	32	29	9
i4	104	98	6	33	31	6
C432	142	107	25	45	38	16
xxx	165	119	28	51	41	20
example2	111	101	9	42	37	12
C880	214	159	26	69	56	19
alu2	251	170	32	74	57	23
i5	168	147	13	56	50	11
C499	260	217	17	79	70	11
C1355	322	235	27	93	74	21
C1908	462	302	35	139	101	27
rot	230	184	20	83	67	19
apex6	287	260	9	110	101	8
alu4	505	336	33	148	111	25
x3	425	345	19	124	105	15
C3540	756	566	25	249	202	19
C6288	1568	917	42	501	296	41
C5315	1125	882	22	358	252	30
Avg.	-	-	20	-	-	18

41% (e.g., C6288). On the average, using our method, the number of cliques is reduced about 20% and the number of sleep transistor is reduced about 18% as compared to the method without considering functionality.

Table 4.2 shows the ratio of gates with multiple fan-out to the total number of gates. From the table, we found that the low reduction ratio of sleep transistor using our method are those circuits that have less percentage of gates with multiple fan-out, i.e., circuits are more likely to have few reconverged paths (e.g., 9symml, i4).

Table 4.3: Ratio of gates with multiple fan-out

Circuits	Gates	Gates (multi_fanout)	ratio(%)
x2	66	10	15
9symml	246	22	9
apex7	268	43	16
i4	270	4	1
C432	287	81	28
xxx	287	81	28
example2	343	48	14
C880	424	122	29
alu2	433	96	22
i5	448	67	15
C499	542	218	40
C1355	590	250	42
C1908	724	281	39
rot	752	150	20
apex6	754	108	14
alu4	830	236	28
x3	1089	77	7
C3540	1426	468	33
C6288	2353	1393	59
C5315	2437	692	28