Chapter 1

Introduction

In CMOS digital circuits, power dissipation consists of dynamic and static power consumption. The average dynamic power consumption is given by Equation (1.1).

$$P_{avg} = \frac{1}{2} V_{dd}^2 f \Sigma_v C(v) \cdot E(v) \tag{1.1}$$

where f is clock frequency, $C(v)$ is the loading capacitance, and $E(v)$ is the switching activity at the output of gate v. With the progress of VLIS process technology, the supply voltage V_{dd} is scaled down to reduce dynamic power and to avoid reliability problems in DSM. However, reducing V_{dd} alone causes the degradation of the circuit's performance. In Equation (1.2), we can see that one way to maintain the performance of circuits is to also scale down the threshold voltage V_{th}.

$$Delay = \frac{C_{load} V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \tag{1.2}$$

Unfortunately, in Equation (1.3) [1], we can see that decrease of the threshold voltage V_{th} will make leakage current increase exponentially. Here, I_0 and V_{off} are constants, while v_t is the thermal voltage (26mV at 300K) and n is the sub-threshold swing parameter. This results in large static power consumption in cut-off region.

$$I_{leakage} = \frac{W}{L} \times I_0 \times e^{(\frac{Vgs - V_{th} - V_{off}}{n \times v_t})} \times (1 - e^{(-\frac{V_{ds}}{v_t})}) \tag{1.3}$$

In the meantime, the diagram shown in Figure 1.1 is an estimated ratio of the static power consumption with the total power consumption when the manufacturing technology is advanced to less than .18 micron. As studied by [2], when the manufacturing technology scales to 0.05 micron in the future, the static power will contribute to nearly 50% of the total power consumption. Therefore, we must put more emphasis on the reduction of static power consumption and related problems.

There are several techniques to reduce leakage power. The first technique is to set the primary inputs of the circuits to the best vector that minimizes power in the sleep mode [3][4][5]. This technique takes the advantage of the fact that leakage current can be affected broadly by input combinations. The

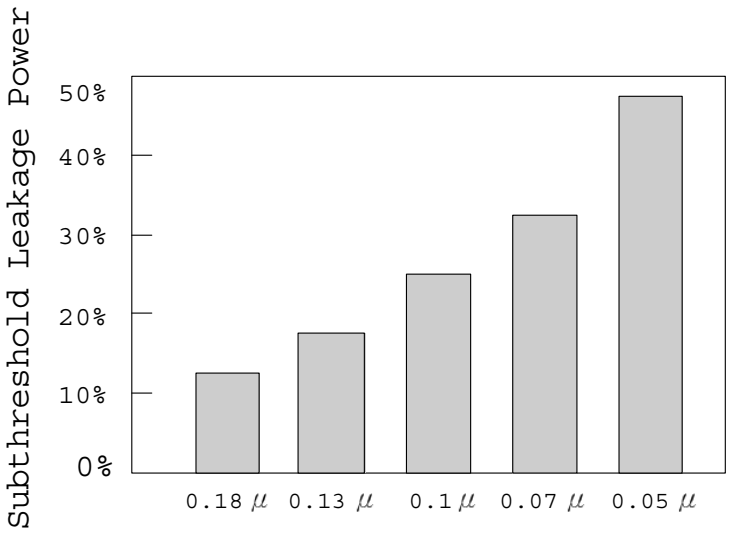

Figure 1.1: Leakage power/total power consumption on different manufacturing technology

challenge is that exhaustively find the best input vector is difficult. Hence, many heuristic approaches were proposed.

The second strategy is to use multiple threshold voltage (multiple-Vth) on a single IC. It uses low-Vth transistors for gates on the critical path and high-Vth transistors on the non-critical path [6]. High-Vth gates have lower static power consumption but cause some performance degradation. Therefore, using high-Vth gates on non-critical paths will achieve significant saving of leakage power without mitigating the performance of the circuits. Using static timing analysis, the slacks of gates can be fully used to get good results. This technique requires only an extra mask layer to select between

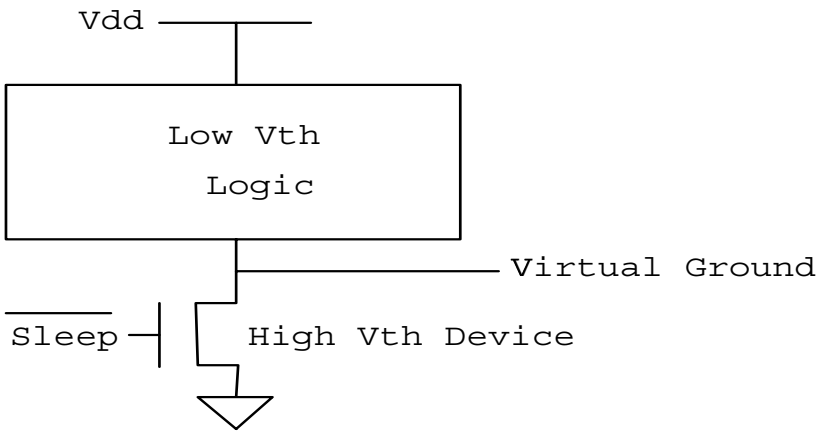

Figure 1.2: MTCMOS circuit structure

high and low threshold voltages.

Another technique is to use a high threshold sleep transistor with a sleep mode called Multi-Threshold CMOS (MTCMOS) [7][8][9][10]. The basic structure is illustrated in Figure 1.2 where reducing the leakage current is during idle mode by providing a high Vth transistor in series with the low Vth circuit transistors. The logic gates are implemented using low Vth devices and are connected to a virtual ground line. This virtual ground line is linked to the true ground rail through a high Vth transistor, called a "sleep transistor". The sleep transistor is controlled by a $SLEEP$ signal for active/standby mode. In active mode ($SLEEP = 0$), the sleep transistor is turned on and the logics operate with sufficient speed through the low Vth device, while in sleep mode ($SLEEP = 1$) the sleep transistor is turned off.

This will cause the virtual ground line to float and reduce the leakage current only from high Vth sleep transistor which is very low. This technique can be realized easily but at the expense of a slight speed loss.

Correct sleep transistor sizing is the key parameter when designing the MTCMOS circuits. The power consumption, area and the performance are affected with each others at the same time. If the sleep transistor size is too large, the circuit performance can be maintained but the dynamic power consumption of the sleep transistor will increase. On the other hand, if the sleep transistor size is too small, there will be significant performance degradation because of the increased resistance to ground. Therefore, designing the size of sleep transistor must take these three factors into consideration. In this thesis, we will propose a method to solve the sleep transistor sizing problem. We take the topology and the functionality of circuits into consideration to minimize the total size of sleep transistors under a specified timing degradation.

The rest of the thesis is organized as follows. Chapter 2 will present the related work and our motivation. Our method will be shown in Chapter 3. Benchmark results are shown in Chapter 4. Finally, conclusion remarks are drawn in Chapter 5.