1. Introduction

More and more digital devices are capable of processing speech, including recording and replay. However, most of them cannot perform speech recognition due to the constraints of weak computational power and lack of floating-point arithmetic. This study tries to overcome these constraints, such that the speech recognition could be used more widely on embedded systems of low-end machines.

1.1 System overview

This study tries to build a speech-recognition system on a 32-bit fixed-point processor. The flowchart for both training and recognition phases is shown in Fig. 1.

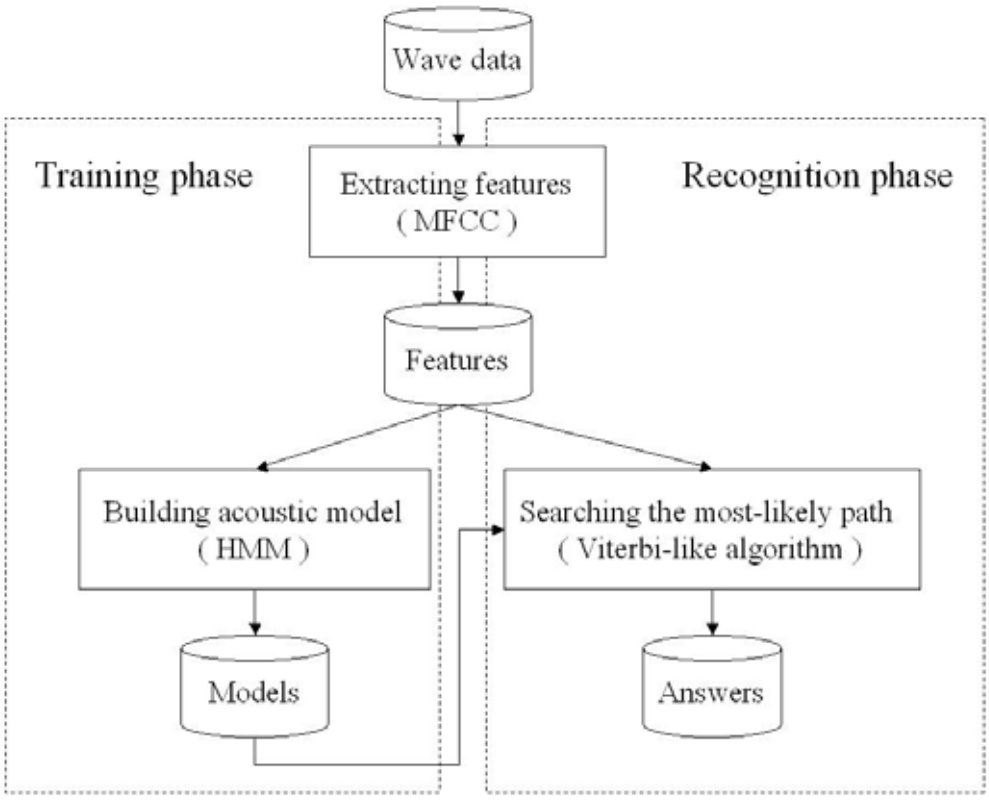

Fig. 1 Flowchart of speech recognition (including training and recognition phases).

The most critical parts of the recognition process lie in feature extraction and recognizer decoding. These two tasks need to be computed on the embedded system, and therefore this study proposes several approaches to accelerate the computation of these two tasks.

1.2 Thesis organization

In the Chap. 2, we introduce previous work on embedded speech recognition.

In the Chap. 3, methods to extract features, build acoustic model and search the most-likely path are introduced. Practical implementation of these methods on embedded system is also discussed.

In the Chap. 4, speed and recognition rates between floating-point and fixed-point computations is compared and discussed. Experimental results of accuracy and parameter estimation are demonstrated.

In the Chap. 5, we give conclusions and list possible future directions to improve the current approach.