Abstract

We describe a gigabit IPv4-IPv6 Translator on a chassis-based platform containing a pair of Vitesse IQ2000 network processor module. It provides an order of magnitude improvement in packet throughput over an implementation of the same functionality on general purpose PC. The next generation Internet Protocol, IPv6, became an Internet Engineering Task Force (IETF) standard in late 1995, motivated by concern that the IPv4 address space would soon be exhausted. The use of classless interdomain routing (CIDR), efficient allocation of address blocks and the use of network address translation (NAT) at the edges has postponed the day expected. However, the depletion of IPv4 address space is inevitable. It is generally agreed that it may take a long time to migrate from IPv4 to IPv6, and that three transition mechanisms, dual stack, tunneling, and address translation will be used. In this thesis, we design an IPv4/IPv6 NAT-PT translator for Network Processor-Based architecture, and implement the system on Chassis-Based Platform. The Network processor has so many advantages like programmability, flexibility, hardware speedup, high speed, and multi-level processing that it can maximize bandwidth utilization and network traffic flow. Moreover, we embedded the Network Processor-Based system, as a module, to the Chassis-Based Platform that is scalable for integrating the other service into the multi-service platform. We expect that our achievement can be used as a prototype of next generation core-network equipment.

中文摘要

因為 IPv4 網路協定位址空間將不敷使用，因此 IETF 已於 1995 年末制訂了新 一代的網際網路協定，稱之為 IPv6。雖然我們利用 CIDR 將位址區塊做有效率的分配，且在網際網路的邊界使用 NAT 的技術來延遲這天的到來，然而，IPv4 網際網路協定位址將不足以提供目前大量的使用者卻是必然的。大家都認為要從 IPv4 網路轉換至 IPv6 網路仍需要一段很長的時間，而在這段期間便需要使用一些轉換的機制來使得 IPv4 網路能夠與 IPv6 網路共存，如 Dual Stack、Tunneling 以及 NAT-PT。本論文以「網路處理器」為開發的平台，來設計與實作上述功能之網路通訊協定轉換器，並將此系統以「模組」的形式嵌入至機架式的網路平台上。網路處理器為一特別針對網路資料處理而設計的處理器，結合軟硬體的優點，達到第三、四甚至第七層封包快速處理的目的，並保有軟體設計時的彈性。其特色在於可以提供「高速」、「強大處理能力」、「高效能」、以及「多層次」等等特色。而機架式的網路平台更具擴充性，可以整合多種網路服務技術成為一向多元化整合服務系統。而本論文之成果，可配合未來網路環境需求，作為下一代核心網路設備之雛形。