APPENDIX A

THE DSP PROGRAM CODE FOR THE SPEED CONTROLLED IPMSM DRIVE

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;~~~DSP program code of the speed controlled IPMSM drive ~~~~~~~~~~~~~~~

;***start general initialization**************
start:    NOP
          NOP
          SETC  INTM; dis. all maskable INT
          LDP   #0;
          SPLK  #0,IMR;   ;mask  maskable INT1-INT6
          LACL   IFR;     ;dis. 6 core maskable INT flags step 1
          SACL   IFR;     ;dis. 6 core maskable INT flags step 2
          SPM    0;
          SETC   SXM; repeat reset init.
          CLRC   OVM; repeat reset init.
          CLRC   CNF; repeat reset init.
;******* AR0 is the stack pointer to addr. 7fh********
          LAR    AR0,#7fh;
;******** start NMI CR setting**********
             LDP    #DP_PF1;
             SPLK   #1,NMICR; falling edge trig NMI;
;---initialize 3 sys. clock source:cpu-20MHz,system-10MHz, WD-15.36ms
             LDP    #DP_PF1;     data page 224
             SPLK   #0043h,CKCR0;  clkin;LPM0;sysclk=cpuclk/2
             SPLK   #00BBh,CKCR1;  clkin=10M;pll=/2*4=20MHz
             SPLK   #00C3h,CKCR0;  enable 20MHz pll
             SPLK   #0100000011000000b,SYSCR;
;----------watch dog timer  setting-----------------
           SPLK   #0000000000101000b,WDCR
             KICK_DOG
;--------be careful after KICK_DOG the DP=0=DP_0-----
             LDP    #DP_VAR;
             SPLK   #0004h,temp;
             OUT    temp,WSGR; set 1 wait state for I/O
             LDP   #DP_PF2; digital I/O Data page
             SPLK  #0030h,OCRB;select QEP1(cap1)
;*********  start ADC1 and 2 settings   *****
        LDP   #DP_PF1;
        SPLK  #0000000000000100b,ADCTRL2;
```

```
;******* start T1 and T2 setting************
            LDP   #DP_EV;  start from:7400h event mang. data page
            SPLK  #1000,T1PR;T=1000x2C*50ns=0.1ms;f=10KHz
            SPLK  #7999,T2PR;T=7999+1=8000
            SPLK  #0,T1CNT                ;clear t1 cnt
            SPLK  #0,T2CNT
            SPLK  #1010100000000000b,T1CON  ;disable t1
            SPLK  #1001100000110000b,T2CON  ;disable t2
            SPLK  #1110010011110000b,CAPCON; for QEP setting
                  SPLK  #1010100001000000b,T1CON  ;start T1 counting
            SPLK  #1001100001110000b,T2CON  ;start T2 counting
      LDP   #DP_EV;
      SPLK  #off500,CMPR1;PWM 1,2 van=0
      SPLK  #off500,CMPR2;PWM 3,4 vbn=0
      SPLK  #off500,CMPR3;PWM 5,6 vcn=0
      SPLK  #0000011001100110b,ACTR;
            ;5432109876543210
      SPLK  #0000100011111000b,DBTCON;
            ;5432109876543210
            ;dead time=3.2us;
      SPLK  #0000001000000111b,COMCON;
      SPLK  #1000001000000111b,COMCON;
;******* for spd. and current loop****
    LDP   #DP_EV;       ;for peripheral setting
    SPLK  #0ffffh,EVIFRA; write 1 to clear all 11 flag regs
    SPLK  #0200h,EVIMRA  ;unmask bit 9:T1UF int
    SPLK  #0,EVIMRB      ;mask all 8 mask regs
    SPLK  #0,EVIMRC      ;mask all 4 mask regs
    LDP   #DP_0; data page=0;  for core setting
    LACL  IFR  ;clear all 6 IFR regs (1)
    SACL  IFR   ;clear all 6 IFR regs (2)
    SPLK  #0002h,IMR;  unmask int2 IMR regs
    CLRC  INTM      ;enable global maskable int switch
;***end of general initialization**************



;*******  main program loop **********
LOOP:       NOP
            KICK_DOG
            CLRC      INTM; for enable INT
            NOP;
          B LOOP;
```

```
;*******   end of main loop*********

      .sect    ".gisr"
NULL:      NOP
           RET
                  ;when T1 underflow(0.1ms), int2 occurs
                  ;start spd. and current loop
;*****************Interrupt vector table for core***********
     .sect   ".vectors"
          B       start           ;00h reset
          B       NULL            ;02h INT1
          B       gisr2           ;04h INT2
          B       NULL           ;06h INT3
          B       NULL            ;08h INT4
          B       NULL            ;0Ah INT5
          B       NULL            ;0Ch INT6
          B       NULL            ;0Eh reserved
          B       NULL            ;10h INT8  user-defined
          B       NULL            ;12h INT9  user-defined
          B       NULL           ;14h INT10 user defined
          B       NULL           ;16h INT11 user defined
          B       NULL           ;18h INT12 user defined
          B       NULL           ;1Ah INT13 user defined
          B       NULL           ;1Ch INT14 user defined
          B       NULL           ;1Eh INT15 user defined
          B       NULL           ;20h INT16 user defined
          B       NULL           ;22h TRAP
          B       nmi_isr          ;24h NMI
          B       NULL           ;26h reserved
          B       NULL           ;28h INT20 user defined
          B       NULL           ;2Ah INT21 user defined
          B       NULL           ;2Ch INT22 user defined
          B       NULL           ;2Eh INT23 user defined
          B       NULL           ;30h INT24 user defined
          B       NULL           ;32h INT25 user defined
          B       NULL           ;34h INT26 user defined
          B       NULL           ;36h INT27 user defined
          B       NULL           ;38h INT28 user defined
          B       NULL           ;3Ah INT29 user defined
          B       NULL           ;3Ch INT30 user defined
          B       NULL           ;3Eh INT31 user defined
;***************all interrupt service routines****************
```